

User Manual



Tektronix Logic Analyzer Family Version 4.0 Software

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:



WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*



CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:



WARNING
High Voltage



Protective Ground
(Earth) Terminal



CAUTION
Refer to Manual



Double
Insulated

Preface

This manual contains operating information for the Tektronix Logic Analyzer family. The manual consists of the following sections:

- *Getting Started.* Provides basic information about installing and using the logic analyzer.
- *Operating Basics.* Provides an overview of the logic analyzer connectors, introduces you to the logic analyzer and pattern generator windows, and explains the basic operation of the Tektronix Logic Analyzer.
- *Reference.* Provides detailed information of the logic analyzer. This section is broken down according to the window types.
- *Appendix A: Specifications.* Lists the environmental, physical, and electrical properties of the logic analyzer family.
- *Appendix B: TLA 700 Symbol File Format.* Provides information on the contents of symbol files using the TLA700 Symbol File format.
- *Appendix C: PG Physical-Logical Conversion.* Provides information on using signals between the LA module, DSO module, and the PG module.
- *Appendix D: TLA700 Module Installation.* Provides installation instructions for logic analyzer modules. Refer to this appendix if you need to install modules in the TLA700 mainframes.
- *Appendix E: Merging Modules.* Provides instructions for merging modules to create wider mainframes for specific applications.
- *Appendix F: Power Cord and Line Fuse Requirements for the Benchtop and Expansion Mainframes.* Provides information on the power and fuse requirements for the benchtop and expansion mainframes.
- *Appendix G: Installing Software.* Provides instructions for reinstalling the system and application software and firmware.
- *Appendix H: User Service.* Provides user service information.

Related Documentation

In addition to this user manual, the following documentation is available for your Tektronix logic analyzer:

- The online help provides information about the user interface and the TLA 700 Programmatic Interface (TPI). To view the online help, select Help Topics from the Help menu.
- The TLA7PG2 online help provides information about the pattern generator user interface and the Pattern Generator Programmatic Interface (PPI). To view the online help, select Help Topics from the Help menu in the TLA7PG2 application.
- The online release notes provide last-minute product and software information not included in this manual. Refer to *Release Notes* on page 1–29 for information on viewing the release notes.
- A series of microprocessor support instruction manuals provide operating and service instructions for the individual microprocessor support packages.
- The *TLA7QS QuickStart Training Manual* provides training exercises to help you learn key features of the logic analyzer. The training manual is designed to be used with the TLA7QS QuickStart training board.
- The *Tektronix Logic Analyzer Family Performance Verification and Adjustment Technical Reference Manual* provides performance verification and adjustment procedures for the major components of the Tektronix logic analyzer.
- A series of service manuals provide board-level service information for the logic analyzer modules and mainframes.
- A series of probe manuals provide detailed instructions for using individual logic analyzer and pattern generator probes.

Terms Used in this Manual

The following terms are used throughout this manual. Refer to the *Glossary* for information on other logic analyzer terminology.

- **LA Module.** An abbreviation and generic term for the logic analyzer module.
- **DSO Module.** An abbreviation and generic term for the oscilloscope module.
- **PG Module.** An abbreviation and generic term for the pattern generator module.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

* This phone number is toll free in North America. After office hours, please leave a voice mail message.
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.



Getting Started

Getting Started

The Tektronix Logic Analyzer family consists of the TLA600 and TLA700 series logic analyzers, and all of the accessories and supports that can be used with them. For more information about availability, contact your Tektronix representative and view the Tektronix website at: www.tektronix.com.

TLA600 Series Logic Analyzers

The TLA600 logic analyzers are a high-performance line of logic analyzers. There are two basic styles: one style has an internal display, and the other uses an external display as shown in Figure 1–1. The TLA600 logic analyzers offer a variety of channel widths and memory depths.

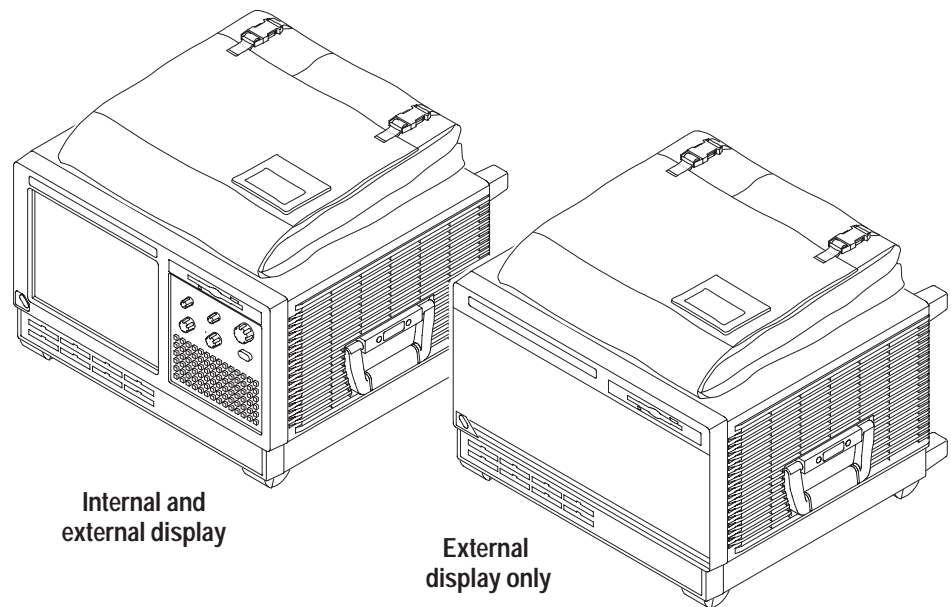


Figure 1–1: TLA600 series logic analyzers

MagniVu, an acquisition technology enabled by the logic analyzers provides 500 picosecond timing resolution on all channels and requires no additional probing.

TLA700 Series Logic Analyzer

The TLA700 series logic analyzers combine a high-performance logic analyzer module with an optional digitizing storage oscilloscope (DSO) module and pattern generator module.

There are two styles of mainframes: portable and benchtop. Each mainframe can also include an expansion mainframe that looks similar to the benchtop mainframe and is compatible with both the portable and benchtop mainframes. The portable mainframe and the benchtop mainframe are shown in Figure 1–2 and Figure 1–3.

Several logic analyzers modules are available in various combinations of channel width and memory depth. All of the logic analyzer modules provide simultaneous state and timing measurements through a single probe.

MagniVu, an acquisition technology enabled by the logic analyzers provides 500 picosecond timing resolution on all channels and requires no additional probing.

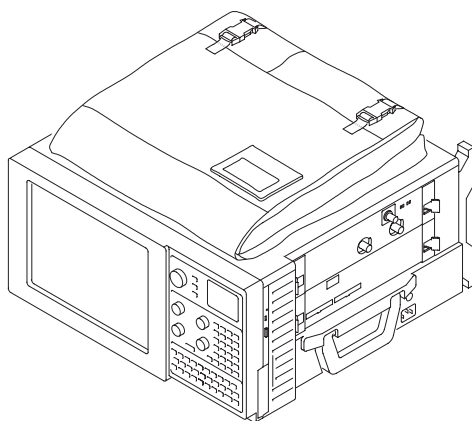


Figure 1–2: TLA700 portable mainframe

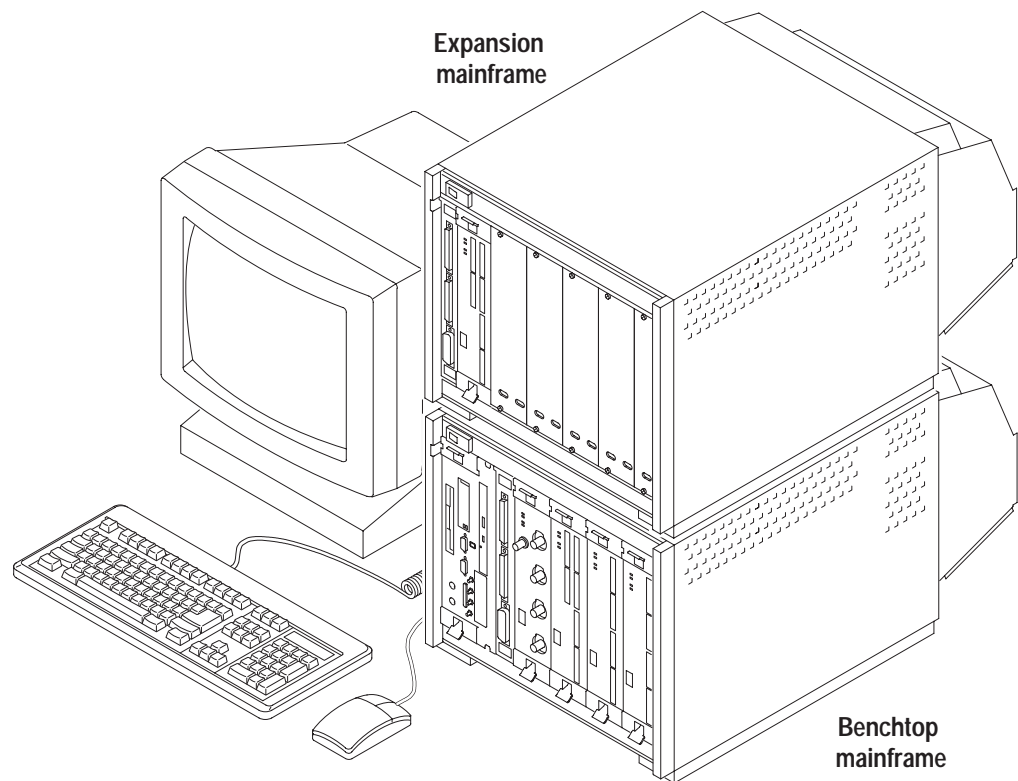


Figure 1–3: TLA700 benchtop mainframe with an expansion mainframe

Acquired data using the digital real-time signal acquisition enabled by the DSO module is time correlated with data from other modules for displays and intermodule triggering and signalling.

The pattern generator module provides multi-channel signals for use in applications such as simulation of missing system elements, erroneous signals for stress testing or extended analysis for stimulating a device under test.

The Windows operating system allows you to install any PC-compatible, third-party hardware and software on the instrument.

Accessories

For a complete list of accessories, refer to the online help. Select the Contents tab and click on the Standard and Optional Accessories icon. Then select one of the topics for more information.

Installation

This section describes the steps needed to install your Tektronix logic analyzer.

Check the Shipping List

Verify that you have received all of the parts of your logic analyzer using the shipping list. You should also verify the following:

- Verify that you have the correct power cords for your geographical area.
- Verify that you have backup copies of the installed software. Store the backup software in a safe location where you can easily retrieve the software for maintenance purposes.
- Verify that you have the correct probes (and modules if you have a TLA700 series logic analyzer).
- Verify that you have all the standard and optional accessories that you ordered.

NOTE. *Keep the software packaging available because you will need it to enter the Windows software registration number when you first turn on the logic analyzer.*

Fill out and send in the customer registration card that is packaged with this manual.

Site Considerations

Read this section before installing the logic analyzer. This section describes site considerations, power requirements, and ground connections for your logic analyzer.



CAUTION. *Ensure a two inch (5.1 cm) clearance at the bottom and sides of the instrument to ensure proper cooling.*

TLA600 and TLA714 Logic Analyzers. You can use the TLA600 and TLA714 logic analyzer on a bench or on a cart in the normal position (on the bottom feet).

You can also use the logic analyzer while it rests on the rear feet. If you use the instrument while it is resting on the rear feet, make sure that you properly route any cables coming out of the rear of the instrument to avoid damaging them.

Benchtop and Expansion Mainframes. The benchtop and expansion mainframes are designed to operate on a bench or in a rackmount environment.

Do not stack more than one expansion mainframe on top of the benchtop mainframe or stack more than one expansion mainframe on top of another expansion mainframe.

If you need to stack more than two benchtop and expansion mainframes, install the mainframes in a rack. Rackmount kits are available from third-party vendors. Please refer to the online help under Standard and Optional Accessories for part numbers on the rackmount kits.



CAUTION. *Because of the size and weight of the benchtop and expansion mainframes use care when lifting or moving the mainframe to avoid personal injury while performing the installation procedures.*

For safety always use two people to lift or move the mainframes.

Installing Expansion Mainframes

This section describes how to install a TLA7XM expansion mainframe. If your logic analyzer does not contain any expansion mainframes, you can skip this section. Observe the following guidelines when installing expansion mainframes:

- Do not stack more than one mainframe on top of another mainframe without a rackmount kit.
- The expansion module must be installed in slot 0 of the expansion mainframe.

NOTE. *Verify that all mainframes are powered off before continuing the installation procedure.*

Installing in a benchtop Mainframe

The expansion module can be installed in any slot of the benchtop mainframe except 0–2, which is reserved for the benchtop controller module. If you are only installing one expansion mainframe, you can install the expansion module in slot 12 to keep the expansion cables out of your way.

NOTE. *If you are installing more than two expansion mainframes, always use a rackmount kit. Do not stack more than one expansion mainframe on top of a benchtop or another expansion mainframe. Contact your local Tektronix representative for information on site considerations for multiple mainframes.*

If you are installing two expansion mainframes, consider installing the two expansion modules next to the benchtop controller module to maximize the number of open slots as shown in Figure 1–5 on page 1–7.

You can configure up to four expansion mainframes with the portable mainframe and up to ten expansion mainframes with a benchtop mainframe.

If the expansion module was not already installed in slot 0 of your expansion mainframe, install it now (refer to *Appendix D: TLA700 Module Installation* for detailed module installation instructions).



CAUTION. Do not use the retaining screws to seat the expansion module. The retaining screws are only for securing the module and reinforcing the grounding. Attempting to seat the expansion module with the retaining screws will damage the chassis.

After seating the modules in place, use a screwdriver to tighten the retaining screws (maximum of 2.5 in-lbs).

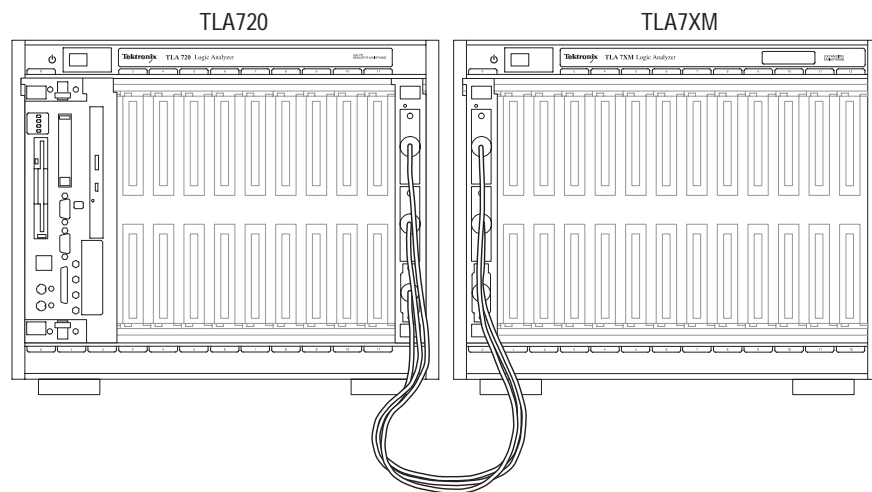


Figure 1–4: Benchtop mainframe and one expansion mainframe

Place the EXPANSION 1 label in the outlined area on the upper right side of the expansion mainframe.

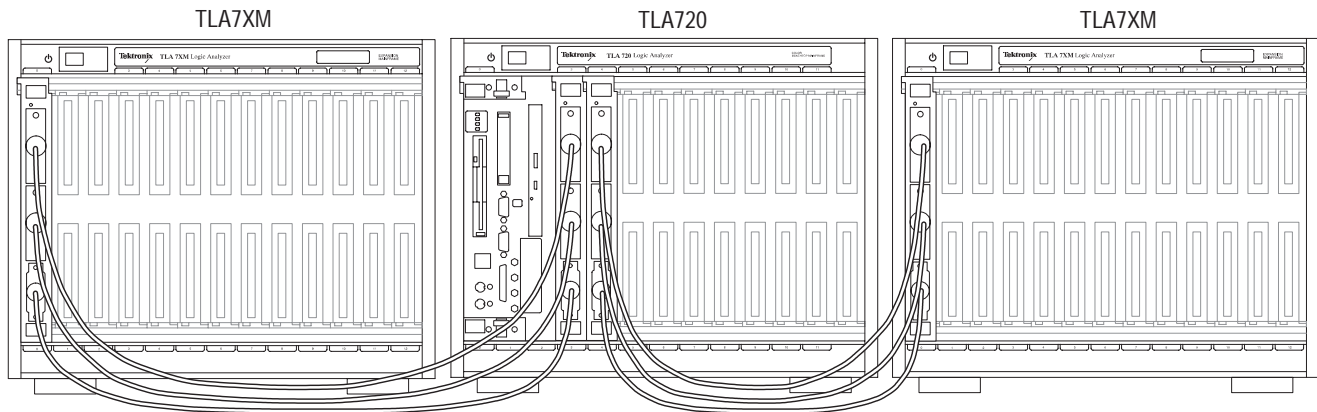


Figure 1-5: Benchtop mainframe and two expansion mainframes

Software determines which expansion chassis is expansion 1 and which is expansion 2 by the order in which the expansion modules are installed in the benchtop mainframe. The expansion module in the lower numbered slot will be expansion 1, and the expansion module in the higher slot will be expansion 2.

For the setup in Figure 1-5 place the EXPANSION 1 label in the outlined area on the upper right side of the expansion mainframe to the left of the benchtop mainframe. Place the EXPANSION 2 label in the outlined area on the upper right side of the expansion mainframe to the right of the benchtop mainframe.

For information on installing modules see *Installing Modules* beginning on page D-1.

Installing in a TLA714 Mainframe

The expansion module can be installed in any slot of the portable mainframe. If you are installing one or two expansion mainframes, you can install the expansion module in slot 1 as shown in Figure 1-6.

If the expansion module was not already installed in slot 0 of your expansion mainframe, install it now.



CAUTION. Do not use the retaining screws to seat the expansion module. The retaining screws are only for securing the module and reinforcing the grounding. Attempting to seat the expansion module with the retaining screws will damage the chassis.

After seating the modules in place, use a screwdriver to tighten the retaining screws (maximum of 2.5 in-lbs).

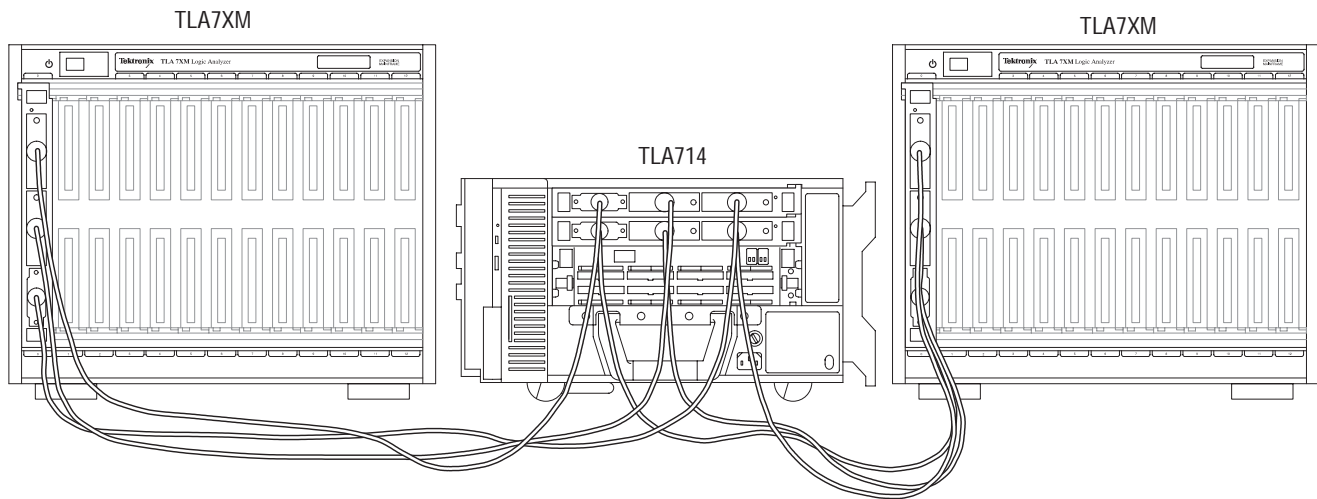


Figure 1–6: Portable mainframe shown with two expansion mainframes

Software determines which expansion chassis is expansion 1 and which is expansion 2 by the order in which the expansion modules are installed. The expansion module in the lower numbered slot will be expansion 1, and the expansion module in the higher slot will be expansion 2.

For the setup in Figure 1–6 place the EXPANSION 1 label in the outlined area on the upper right side of the expansion mainframe to the left of the portable mainframe. Place the EXPANSION 2 label in the outlined area on the upper right side of the expansion mainframe to the right of the portable mainframe.

For information on installing modules see *Installing Modules* beginning on page D–1.

Installing the Expansion Cables

There are three cables that connect the expansion modules together. To connect the expansion modules together, perform the following procedures.

1. Examine the gray expansion cable to determine if the connectors have labels. If the connectors are not labeled, apply the C labels to each connector.
2. Connect one end of the gray expansion cable to connector C of the expansion module on the expansion mainframe side. Connect the other end of the gray expansion cable to connector C of the expansion module on the benchtop or portable mainframe side.
3. Fasten the expansion cable connector to the expansion module by tightening the two hold down screws.



CAUTION. Do not use the hold down screws to seat the expansion cable. The hold down screws are only for securing the cable to the module and reinforcing the grounding. Attempting to seat the expansion cable with the hold down screws will damage the connectors on the chassis.

4. Examine the two blue expansion cables to determine if the connectors are labeled A and B. If the cables are labeled A and B, select the B cable and proceed to step 6.
5. If the cables are not labeled, select either blue expansion cable and label each connector with the B label. Select the other cable and apply the A labels to each connector.
6. Connect one end of the blue expansion cable to connector B of the expansion module on the expansion mainframe side. Connect the other end of the blue expansion cable to connector B of the expansion module on the benchtop or portable mainframe side.
7. Fasten the expansion cable connector to the expansion module by tightening the two hold down screws.
8. Connect one end of the blue expansion cable to connector A of the expansion module on the expansion mainframe side. Connect the other end of the blue expansion cable to connector A of the expansion module on the benchtop or portable mainframe side.
9. Fasten the expansion cable connector to the expansion module by tightening the two hold down screws.

Installing TLA 700 Modules

If you need to install additional modules for the TLA700 series logic analyzers, refer to *Appendix D: TLA700 Module Installation* for detailed instructions.

Connecting Accessories

After installing the mainframes and modules, you can connect the accessories such as external monitors, keyboard, and printer.

Connecting Accessories to the TLA600 Series

The accessory connections are the same as those you would make on a personal computer. Connect the accessories to the rear of the instrument. The connection points are shown in Figure 1–7.

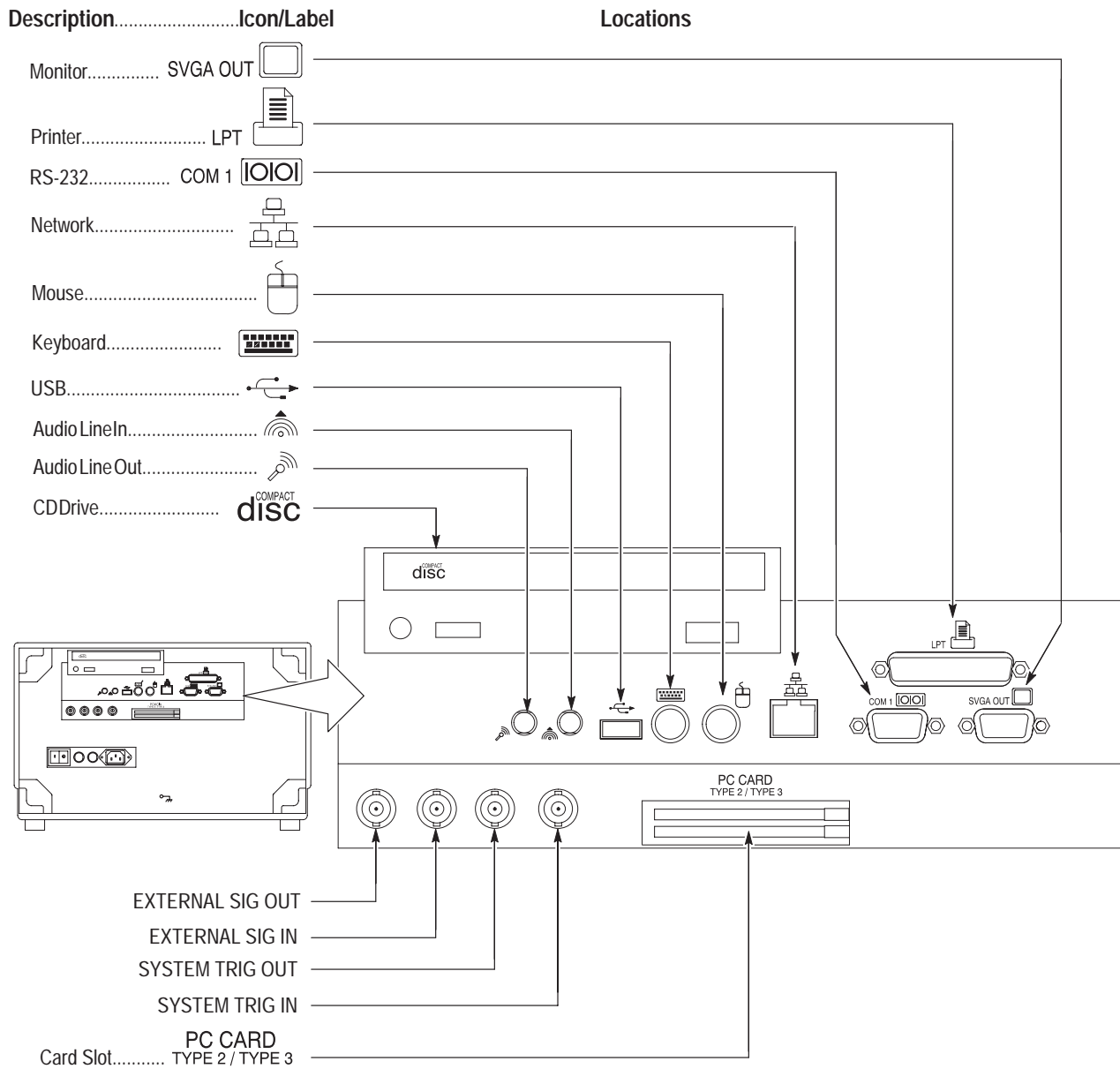


Figure 1–7: TLA600 series accessories connections

Connecting Accessories to the TLA700 Series

The accessory connections are the same as those you would make on a personal computer. The connection points are shown in Figure 1–8. Use the icons that appear in the circled areas as a guide.

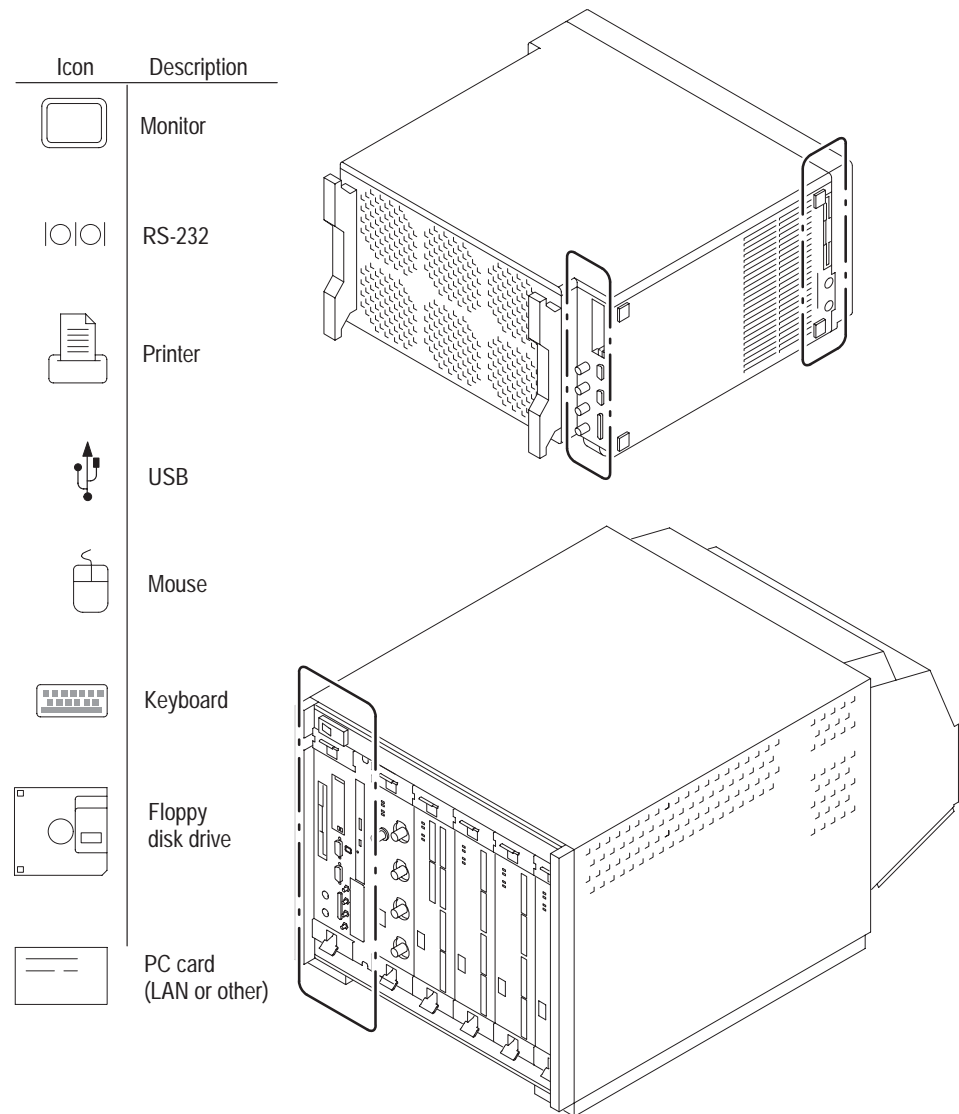


Figure 1–8: TLA700 series accessories connections

Additional Accessory Connection Information

Table 1–1 provides additional information on accessories.

Table 1–1: Additional accessory connection information

Item	Description
Monitor	If you use a non-standard monitor, you may need to change the the Windows display settings to achieve the proper resolution.
Printer	Connect the printer to the ECP (enhanced parallel port) connector directly. If your printer has a DB–25 connector, use the adapter cable that came with your logic analyzer to connect to the ECP connector.

Connecting Probes

After you have connected all of the accessories, you should now connect the probes to the instrument. Refer to the appropriate section for your instrument.

For additional information on the individual probes, refer to the instructions that came with your probes.

Connecting Probes to the TLA600 Logic Analyzer

Connect the logic analyzer probes and the optional retaining brackets as shown in Figure 1–9.

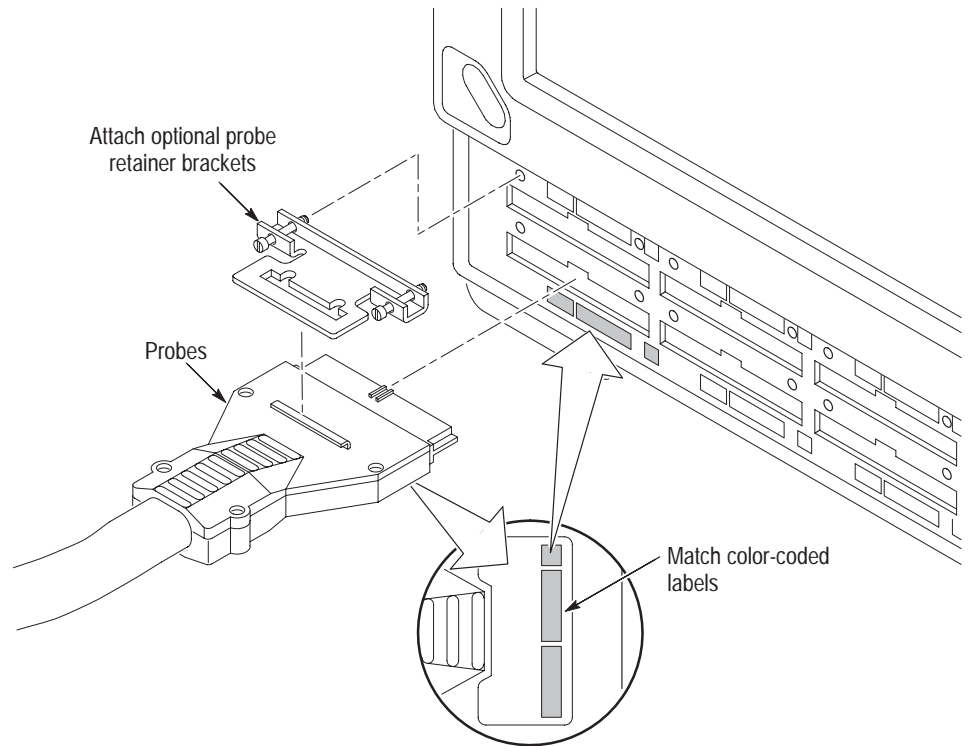


Figure 1–9: Connecting the logic analyzer probes to a TLA600 logic analyzer

Connecting Probes to the TLA700 LA Module

Connect the logic analyzer probes and the optional retaining brackets as shown in Figure 1–10.

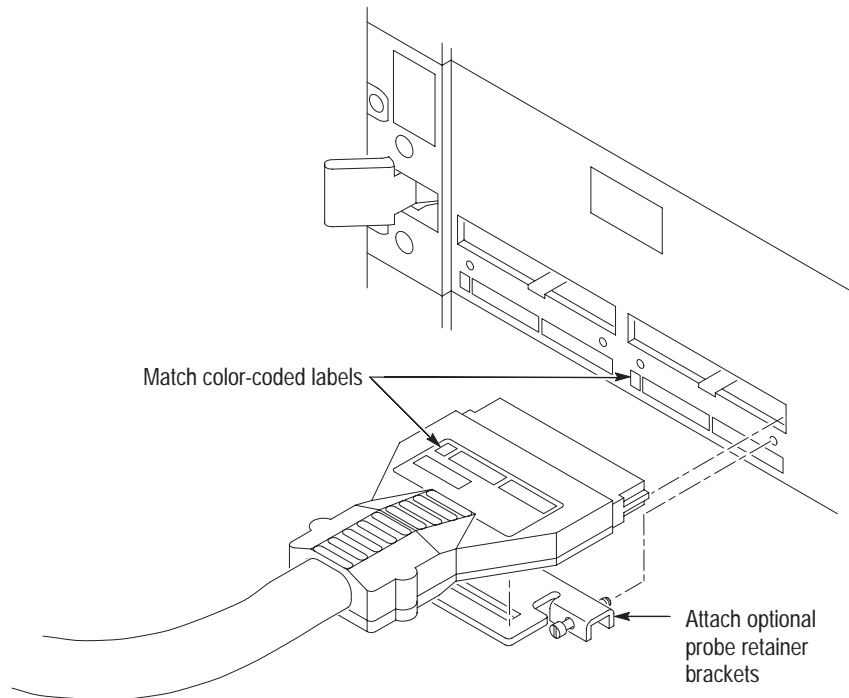


Figure 1–10: Connecting the logic analyzer probes to a TLA700 module

Configuring the P6470 Pattern Generator Probe

The P6470 TTL/CMOS probe comes standard with a 75 Ω series termination resistor pack. This provides impedance matching for the pattern generator and the system under test. Determine the impedance matching for your application and then use the following steps to change the series termination resistors (use the optional 015-A095-00 kit with 2 each of 43 Ω , 75 Ω , 100 Ω , and 150 Ω resistor packs).

To change the resistor packs, do the following:

NOTE. Power down the instrument and disconnect the pattern generator probes from the pattern generator module before changing the resistor packs.

1. Unscrew the 4 screws holding together the probe's case.
2. Push in the holes at both sides of the probe case with a small screwdriver to unlock the latches and pull apart the two sides of the case.
3. Remove the two blue resistor packs, R910 and R900 on Figure 1–11.

4. Insert the two replacement resistor packs.
5. Put together the case and secure it with the 4 screws.

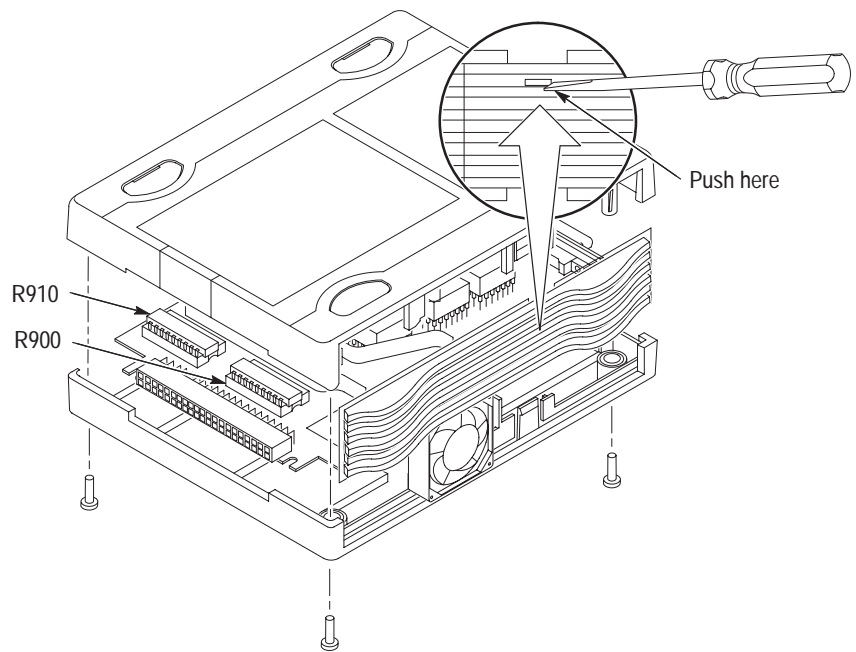


Figure 1-11: Reconfiguring the P6470 TTL/CMOS probe

Connecting the Pattern Generator Probes

Power down the logic analyzer before connecting the pattern generator probe.

Connect the pattern generator probe as shown in Figure 1-12. The probe cable is reversible. You can connect the probe cable in either direction.



CAUTION. To prevent damage to the pattern generator module or probe, do not connect or disconnect the probe cables while the logic analyzer is powered on.

Although the pattern generator probe cable appears to be a SCSI cable, it is not compatible with a SCSI cable; do not use a SCSI cable with the pattern generator module, or use the pattern generator probe cable with a SCSI instrument.

The probe is fragile, handle carefully.

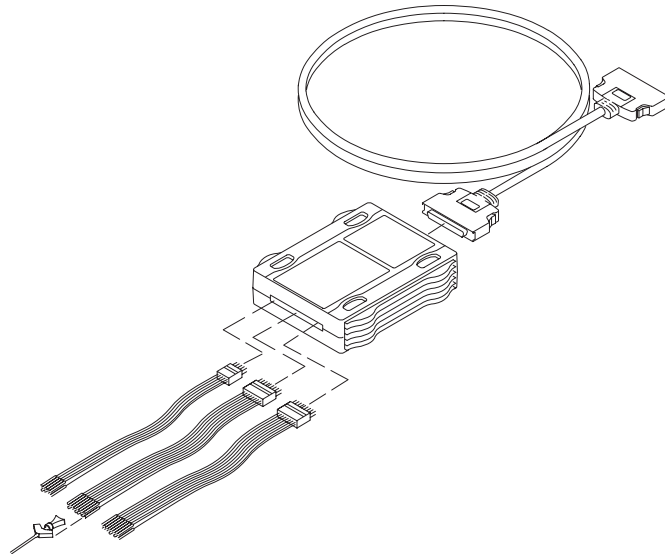


Figure 1-12: Connecting the pattern generator probes

First Time Operation

The first time your logic analyzer is turned on, you will see a TLA Final Setup icon on your desktop. Double click the icon to launch the application for the first time. The TLA application will automatically start every time you power on the instrument.

If you have a TLA700 series logic analyzer with a pattern generator software and module installed, the pattern generator application will also automatically start.

Turning On the TLA600 Series Logic Analyzer

Follow these steps to turn on the logic analyzer for the first time:



CAUTION. *Connect the keyboard, mouse, and other accessories before applying power to the logic analyzer.*

Connecting the accessories after turning on the logic analyzer can damage the accessories.

1. Check that the line fuses are correct for your application. The instrument uses two fuses; both fuses must be the same. See Table 1-2.

Table 1-2: TLA600 series line fuses

Line voltage	Rating	Tektronix part number
90 V to 132 V operation	8 A, fast blow, 250 V	159-0046-xx
207 V to 250 V operation	6.3 A, fast blow, 250 V	159-0381-xx

2. Connect the power cord. See Figure 1–13.
3. If you have an external monitor, connect the power cord and turn on the monitor.

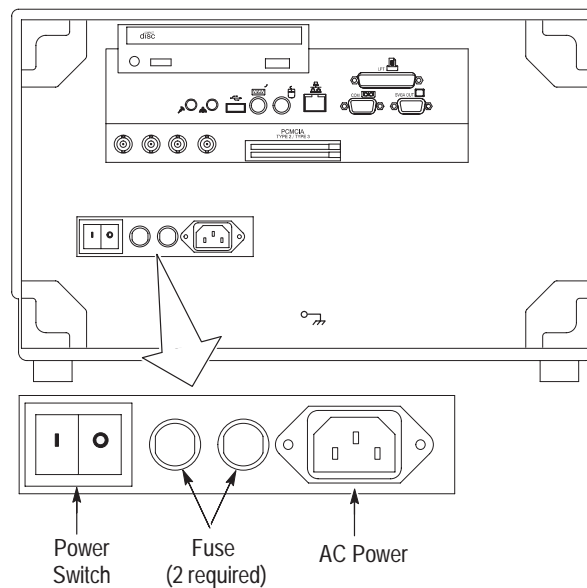


Figure 1-13: Line fuse and power cord connector locations

4. Turn on the logic analyzer as follows:
 - a. Press the On/Standby switch to turn on the logic analyzer (see Figure 1–14 for the switch location).
 - b. Wait for the logic analyzer to complete power-on self-tests, start Windows, and start the TLA application.

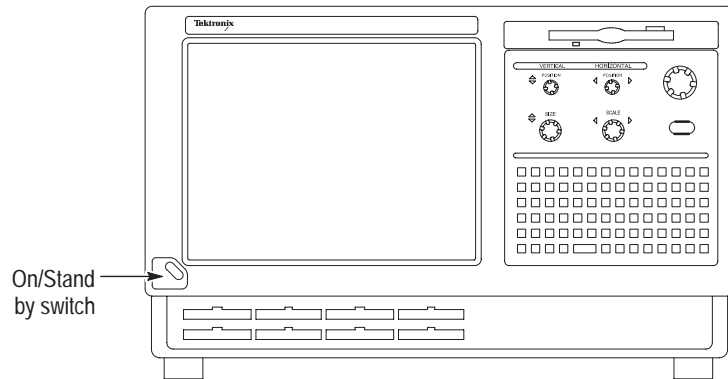


Figure 1-14: On/Standby switch locations

Turning On the TLA700 Series Logic Analyzer

Follow these steps to turn on the logic analyzer for the first time:



CAUTION. Connect the keyboard, mouse, and other accessories before applying power to the mainframe.

Connecting the accessories after turning on the mainframe can damage the accessories.

1. Check that the line fuse is correct for your application. See Table 1-3.
2. Connect the power cord. See Figure 1-15.
3. If you have an external monitor, connect the power cord and turn on the monitor.

Table 1-3: TLA700 series line fuses

Line voltage	Rating	Tektronix part number
Portable mainframe		
90 V to 132 V operation	8 A, fast blow, 250 V	159-0046-xx
207 V to 250 V operation	6.3 A, fast blow, 250 V	159-0381-xx
Benchtop mainframe		
90 V to 132 V operation	20 A, slow blow, 250 V	159-0379-xx
103 V to 250 V operation	15 A, fast blow, 125 V	159-0256-xx
207 V to 250 V operation	6.3 A, fast blow, 250 V	159-0381-xx

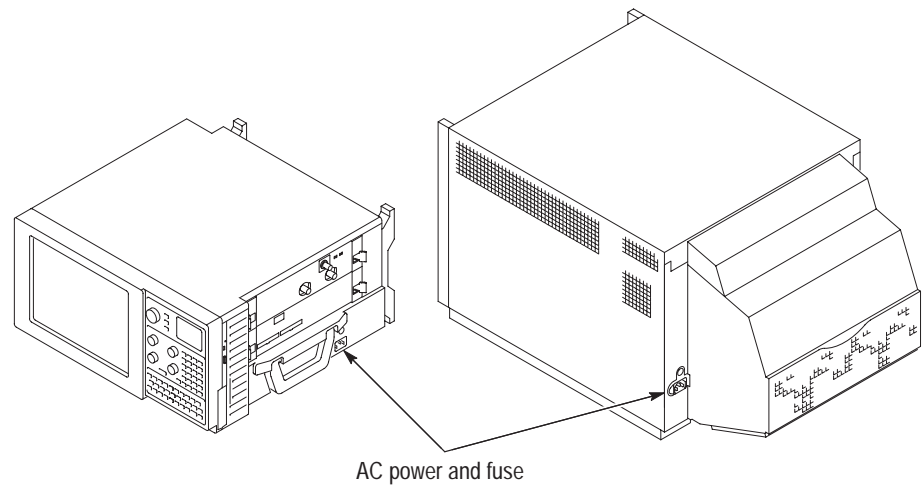


Figure 1-15: Line fuse and power cord connector locations



CAUTION. Although the benchtop mainframe can use the power cord with the 15 A plug, mainframes operating at low line (90 VAC) with four or more instrument modules may require the power cord with the 20 A plug.

If you have four or more modules in your mainframe, you must determine the correct fuse and power cord combination to avoid overloading the power distribution system.

See Power Cord and Line Fuse Requirements for the Benchtop Mainframe for further information.

4. Turn on the mainframe as follows:
 - a. Press the On/Standby switch to turn on the mainframe (see Figure 1-16 for the switch location).
 - b. Wait for the mainframe to complete power-on self-tests, start Windows, and start the TLA700 application.

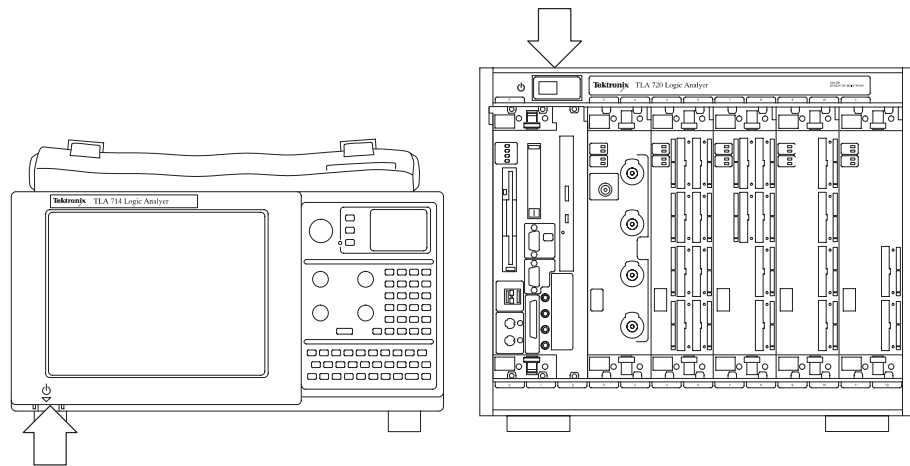


Figure 1-16: On/Standby switch locations

Powering On the Mainframes

The expansion mainframe automatically powers on when the connected benchtop or portable mainframe powers on. If everything is properly connected and operational, you should see the expansion mainframe and the installed modules in the System window.

If the expansion mainframe and the installed modules do not display in the System window, see the Table H-1 beginning on page H-8.

NOTE. You must have a module installed in the expansion mainframe before the expansion mainframe is recognized by the resource manager and appears in the System window.

Turning Off the TLA700 Series Mainframe

Both the TLA714 portable mainframe and the TLA720 benchtop mainframe have a built-in soft power-down function that safely powers down the mainframe when you press the On/Standby switch.

You can set the shutdown mode in the Mainframe Utilities tool in the Windows control panel.

The expansion mainframe automatically powers down when the benchtop or portable mainframe is turned off.

Performing the Incoming Inspection

Incoming inspection consists of verifying the basic operation of the logic analyzer. The power-on diagnostics check the basic functionality. These diagnostics run every time you turn on the logic analyzer.

You can also verify more detailed functionality by running the self calibration and extended diagnostics.

NOTE. Allow the mainframe and modules to warm up for 30 minutes before running the self calibration.

Disconnect any probes attached to the modules. Then select the System menu, and point to Calibration and Diagnostics. Run the self calibration followed by the extended diagnostics by selecting the proper tab. Results of the tests display on the individual property page.

If you are using a pattern generator, select the Pattern Generator System menu and point to Calibration and Diagnostics. Run the self calibration followed by the extended diagnostics by selecting the proper tab. Results of the tests display on the individual property page.

NOTE. The time required to run the self calibration on the logic analyzer modules depends on the number of acquisition channels.

Modules with a large number of channels may take several minutes to run the self calibration.

Checking the Logic Analyzer Probes (Optional)

Connect the logic analyzer probes to a signal source, start an acquisition, and verify that the acquired data is displayed in either the listing or waveform windows.

NOTE. If you connect probes to any channels besides the A2 and A3 groups, you must define the groups and channels in the Setup window before acquiring data on other probe channels.

- Checking the DSO Probes (Optional)** Connect the oscilloscope probes to the Probe Compensation connector on the front panel of the DSO module. You can then run the Calibrate Probe function in each vertical setup page for the module.
- Checking the Pattern Generator Probes (Optional)** Set up a simple pattern generator program to output a signal to the probes. Connect an oscilloscope probe to the probe outputs and verify that the signal is present at the probe outputs.
- Checking the Mainframe (Optional)** To check the mainframe diagnostics not covered by the TLA Application software. Run the QA+Win32 diagnostics or the TLA700 Mainframe Diagnostics located under the Windows Start menu under the Tektronix TLA700 programs. Exit the TLA Application before running the external diagnostics.

Backing Up User Files

Back up your user files on a regular basis. Use the Windows back up tools or copy the files to floppy disks, to a network drive, or to another media. Always keep a backup copy of files that you access on a regular basis.

Removing the Replaceable Hard Disk Drive (TLA700 Series Only)



CAUTION. Do not remove the hard disk drive while the instrument is powered on. Always power down the instrument before removing the hard disk drive.

The hard disk drive can be permanently damaged if you remove it while the instrument is powered on.

Verify that the instrument is turned off.

Remove the replaceable hard disk drive cartridge by depressing it to release the latch. Pull on the replaceable hard disk drive cartridge to remove it from the chassis. Figures 1–17, 1–18, and 1–19 show the procedures for removing the hard disk drive for the benchtop controller and for the portable mainframe. The TLA600 series do not have replaceable hard disk drives.

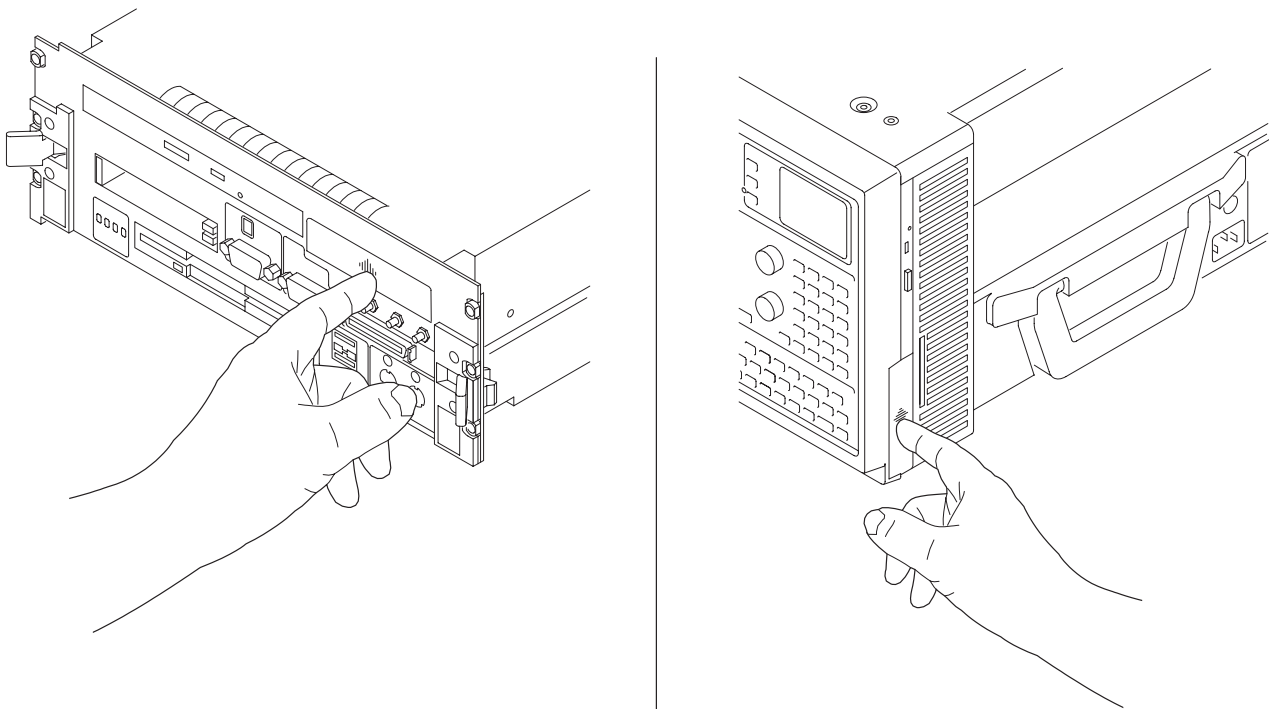


Figure 1–17: Depress the hard disk drive latch

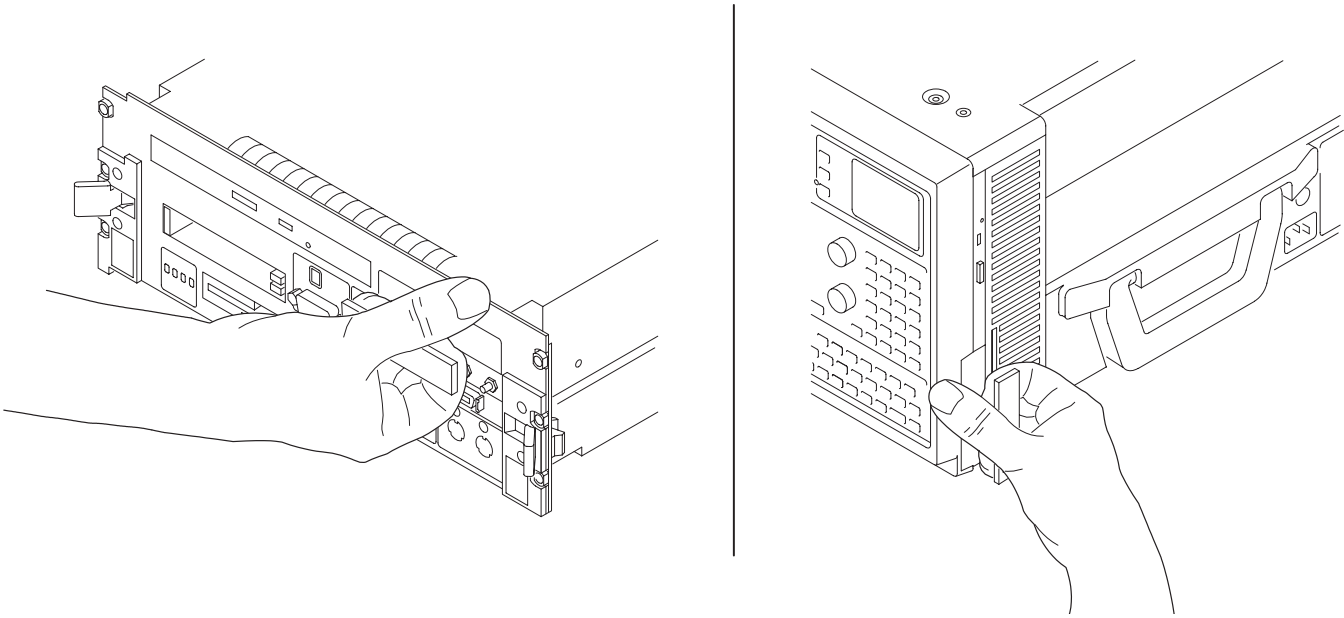


Figure 1-18: Unlatching the hard disk drive cartridge

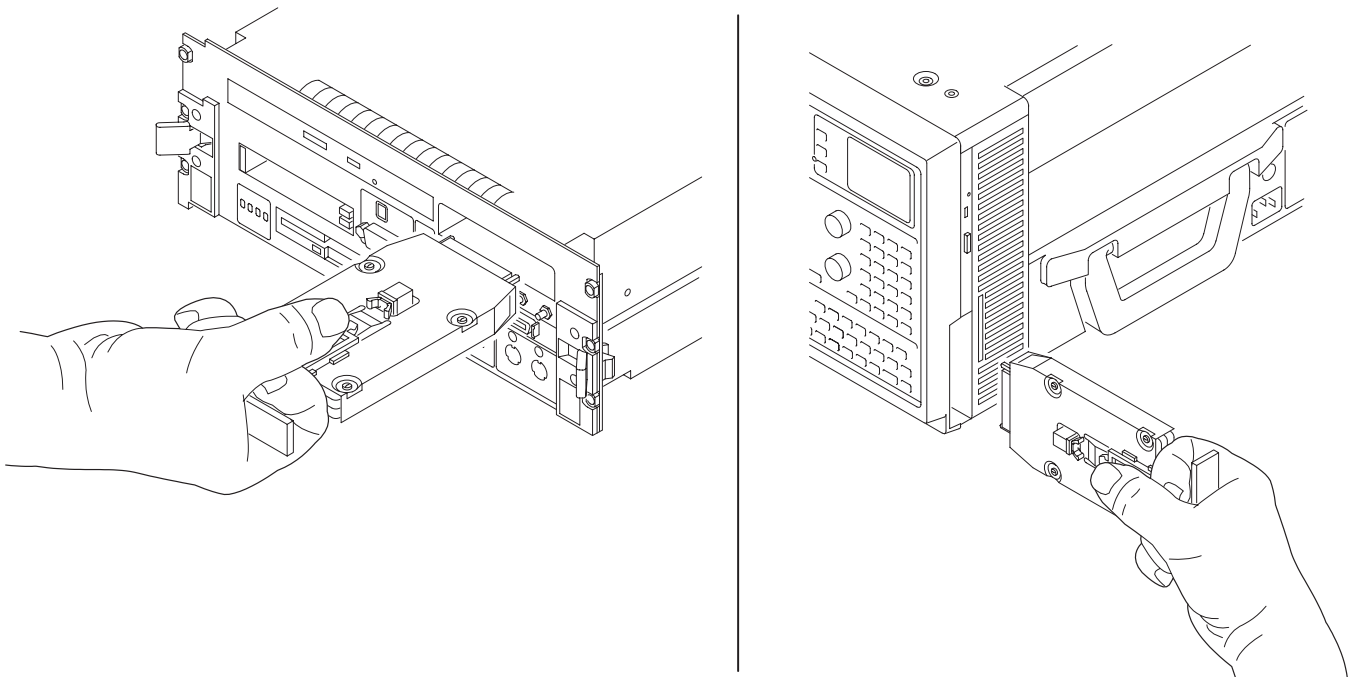


Figure 1-19: Removing the hard disk drive cartridge

Connecting Probes to the Target System

The logic analyzer connects to the target system through probes. The LA probes allow you to connect to the target system in several different ways as shown in the following illustrations. You can use the color-coded probe channels to map the hardware connections to the channel settings in the LA Setup window. Each LA probe group consists of eight channels that can be individually named in the LA Setup menu.

NOTE. *Power off the target system and the logic analyzer before connecting the probes to the target system.*

Connect the probes to the logic analyzer by matching the color-coded label to the label on the LA module. To provide a secure connection to the LA module, you can optionally use the probe retainer bracket with the probe connector.

General Purpose Connections

The P6417 and P6418 probes provide a means to connect to the target system for most applications. Figure 1–20 shows different ways to connect the probe to the target system.

Note the location of the ground connections for the probe:

- The individual podlets have the ground (GND) engraved on the podlet.
- When you use the 8-channel lead sets, the ground lead is a single black connector. Make sure you connect the ground side of the 8-channel lead set to the ground side of the 8-channel podlet holder.

Refer to the *P6417 & P6418 Logic Analyzer Probe Instructions* for information on dimensions for the P6417 and P6418 probes.

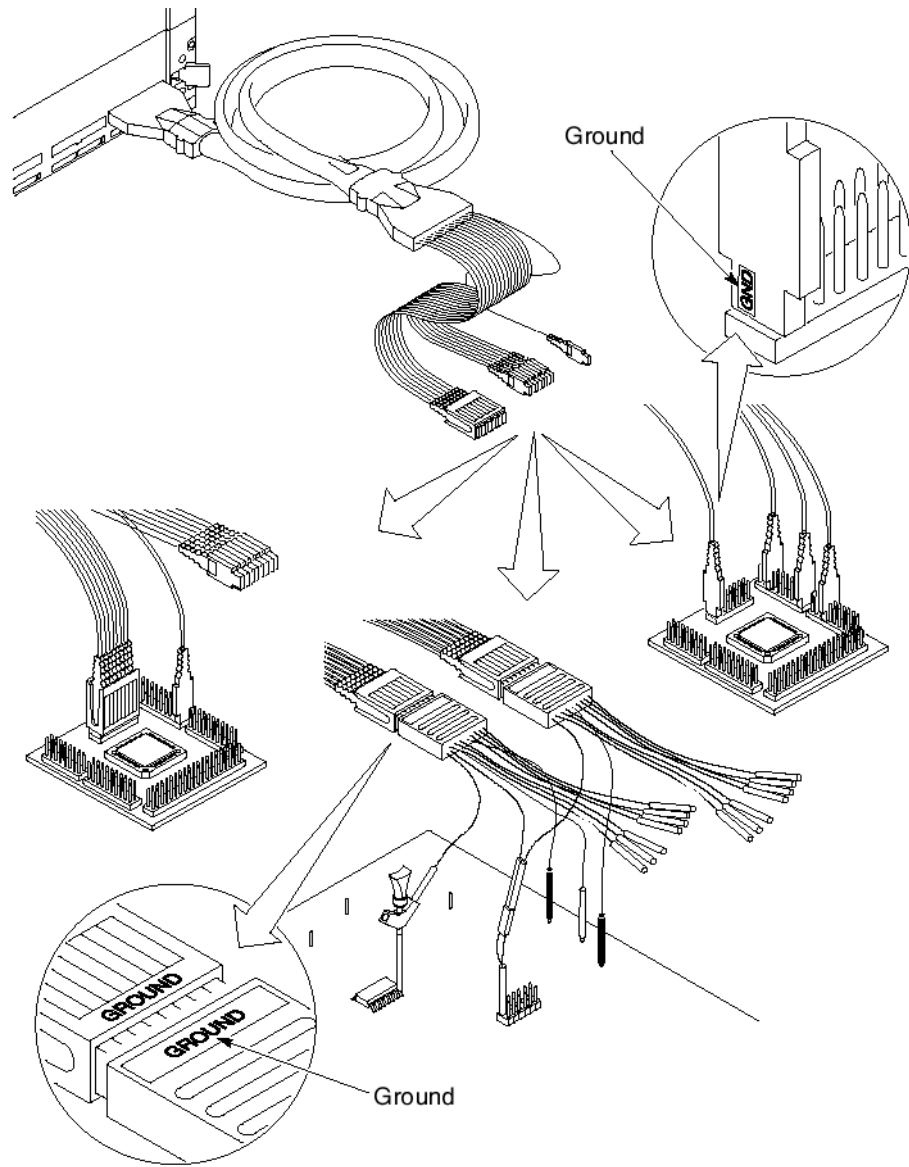


Figure 1-20: 17-channel general purpose probe

High-Density Probe Connections

The P6434 Mass Termination Probe allows you to connect 34 LA channels to a microprocessor probe adapter or directly to the target system. To connect to the target system directly, you must include compatible Mictor connectors in your circuit board design.

Figure 1–21 shows two ways of connecting the LA module to a target system. For more information on the P6434 Mass Termination Probe and how to connect it to your target system, refer to the *P6434 Mass Termination Probe Instructions*.

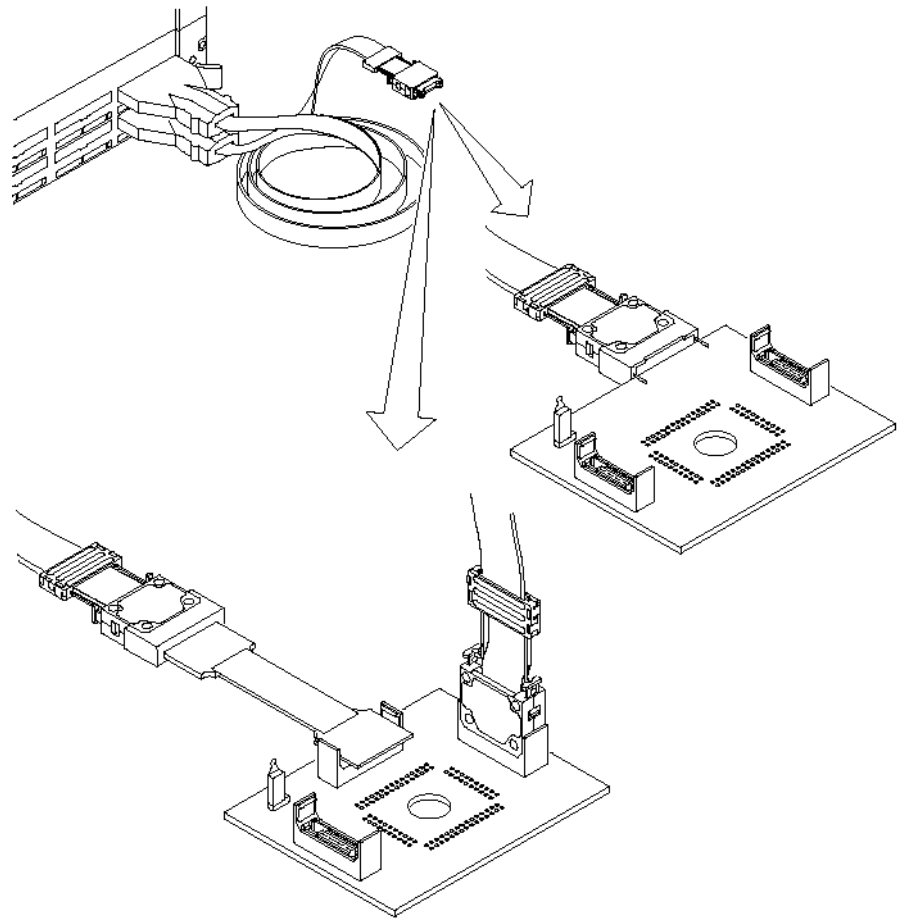


Figure 1–21: P6434 high-density probe connections

Microprocessor Connections

All LA probes can be connected to microprocessor adapters. Refer to the documentation that comes with your microprocessor disassembler package for details about connecting the probes to the microprocessor adapters and to the target system.

DSO Probe Connections Refer to the user documentation that came with your DSO probes (P6243 and P6245 probes) for connecting and using the DSO probes.

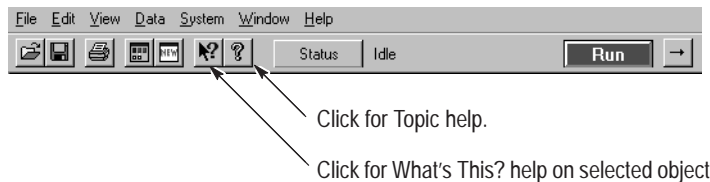
Pattern Generator Probes Refer to the *P6470 & P6471 Pattern Generator Probe Instruction Manual* for more information on using the pattern generator probes with the pattern generator module.

Additional Information

This section lists sources for you to get more information.

Online Help The online help gives detailed information about the logic analyzer and its modules. Look in the online help for details about user interface selections that are not described in this manual. The online help also has basic operating information for microprocessor support products.

To access online help, go to the Help menu, or click the toolbar buttons shown:



Help Topics. Help topics tell you how to perform tasks and describe software features and selections shown on the screen. There are two types of help topics: overview topics and task topics.

Overview topics describe application features, such as the different application windows. Overview topics also describe concepts. Overview topics are available through the Help menu and through Help buttons in dialog boxes. From the Help menu, click Help Topics, and locate the topic using the Contents or Index tab. The Help on Window selection in the Help menu provides overview help for the currently-selected window.

Task topics provide procedure information about how to perform specific tasks. Task topics are available through the Help menu. From the Help menu, click Help Topics, and locate the topic using the Contents or Index tab.

What's This? Help. What's This? help provides a short description of the control or screen feature selected. First click the What's This? button on the toolbar, and then click the item of interest. For further information about the item, go to the Topic help.

TPI Online Help. Select Help on TPI from the drop-down help menu for information on using the TLA Programmatic Interface. A printable version of the TPI online help is available on the instrument. Select Start > Programs > Tektronix Logic Analyzer > TLA Documentation > TPI Manual.

Pattern Generator Online Help. Select Help on TLA7PG2 from the drop-down help menu for information on using the TLA Pattern Generator.

PPI Online Help. Select Help on the TLA7PG2 PPI from the drop-down help menu for information on using the TLA Pattern Generator. A printable version of the PPI online help is available on the instrument. Select Start > Programs > Tektronix Pattern Generator > Pattern Generator Documentation > PPI Manual.

To access the Logic Analyzer Release Notes, select Start > Programs > Tektronix Logic Analyzer > TLA Release Notes.

Windows Online Help. Information about Windows features is available through the Windows help system. Access Windows help as you would with any Windows application.

Release Notes

The online Release Notes contain information about this release of the logic analyzer application and pattern generator application. Check the Release Notes for information such as software compatibility and software version differences from earlier releases.

To access the Logic Analyzer Release Notes, select Start > Programs > Tektronix Logic Analyzer > TLA Release Notes.

To access the Pattern Generator Release Notes, select Start > Programs > Tektronix Pattern Generator > Pattern Generator Release Notes.



Operating Basics

Functional Overview

This chapter is divided into the following sections:

- *Functional Overview.* Provides an overview of the front panel controls of the logic analyzer and the location of external connectors.
- *Approaching the Tektronix Logic Analyzer Windows.* Provides a high-level overview of the basic logic analyzer and DSO windows.
- *Approaching the Pattern Generator Windows.* Provides a high-level overview of the basic pattern generator windows.
- *Operating Basics.* Provides an overview of the logic analyzer operation.

Front Panel Controls

This section introduces you to the front panel controls of the TLA600 series logic analyzer and the color portable mainframe. It provides a brief overview on how to use the front panel controls.

In addition to the front panel controls, you can also control the logic analyzer from an attached keyboard and mouse.

TLA600 Front Panel Controls

For the TLA61X and TLA62X you can use the front panel keys as an alternative to an external keyboard. Most keys and key combinations are available using the front panel. See Figure 2-1.

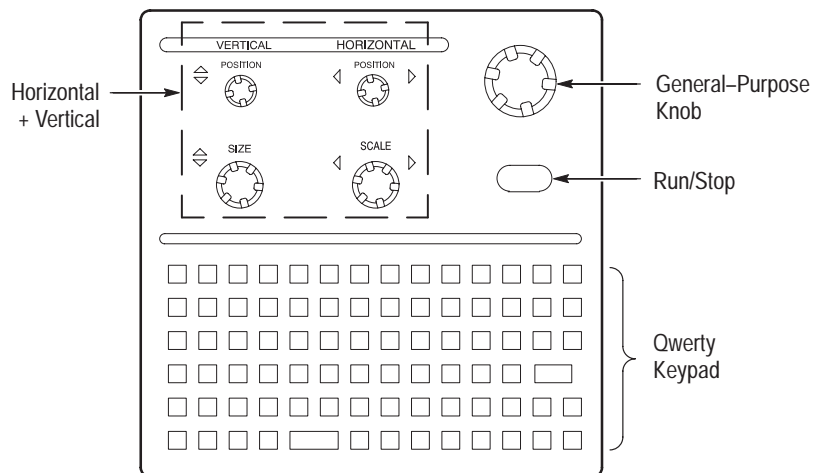


Figure 2-1: Logic analyzer front panel

For key combinations, it is not necessary to hold down more than one key at a time. For example, you can press the SHIFT key in the hexadecimal keypad, and then press a keypad key to accomplish a Shift+key combination. The same is true for other key combinations, such as CTRL and ALT keys.

Portable Mainframe Front Panel Controls

The portable mainframe has front panel controls that operate the logic analyzer without an external mouse or keyboard.

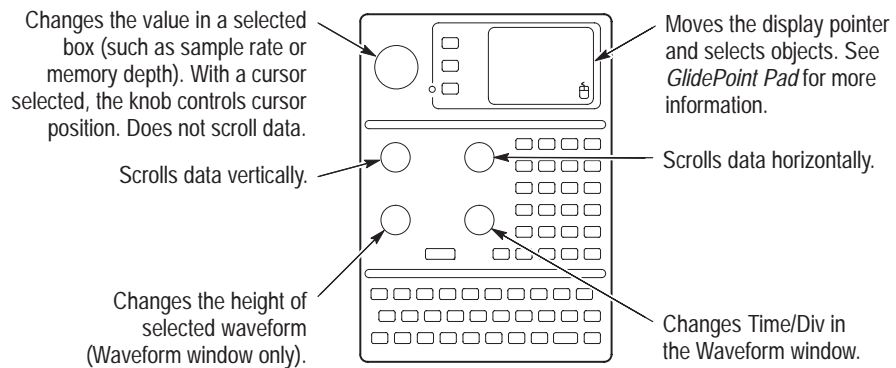


Figure 2-2: Portable mainframe front panel

Keyboard. For the portable mainframe, you can use the front panel keys as an alternative to an external keyboard. Most keys and key combinations are available using the front panel.

For key combinations, it is not necessary to hold down more than one key at a time. For example, you can press the SHIFT key in the hexadecimal keypad, and then press a keypad key to accomplish a Shift+key combination. The same is true for other key combinations, such as CTRL and ALT keys.

Glidepoint Pad. The Color Portable Mainframe has a GlidePoint pad as an alternative to the mouse. To move the pointer, slide your finger lightly over the surface of the pad. Tap the surface to simulate a click of the left mouse button, or use the control buttons to select the type of operation.

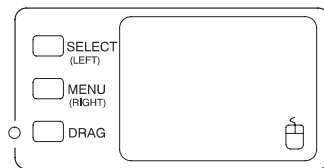


Figure 2-3: GlidePoint pad

TLA600 Series External Connectors

The external connectors on the rear panel of the TLA600 series logic analyzer are shown in Figure 2-4.

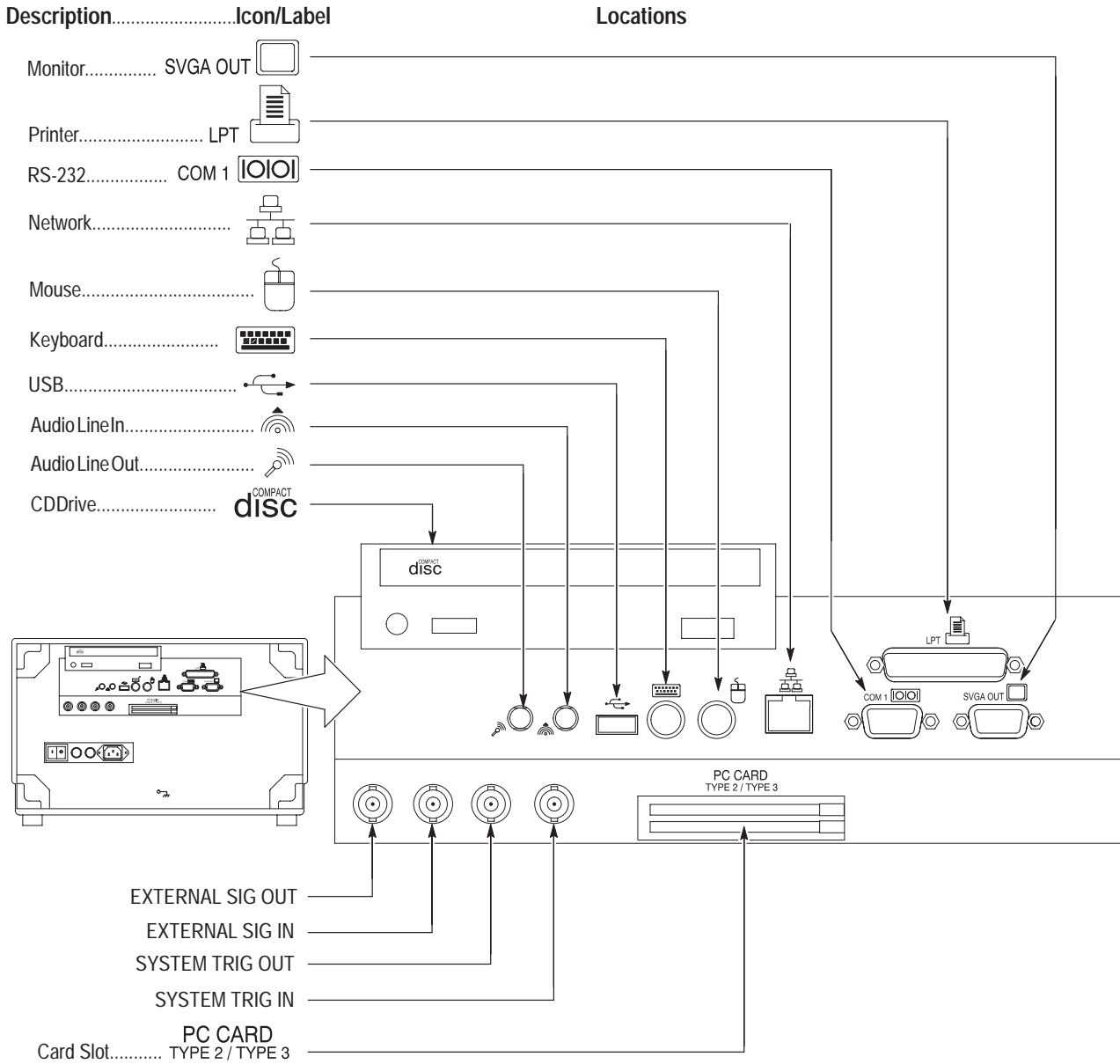


Figure 2-4: TLA600 series external connectors

TLA600 Series Chassis Ground Connections

Figure 2–5 shows chassis ground connections. Use the chassis ground connections to connect the grounds of the target system (system-under-test) to the logic analyzer to ensure a common ground connection between instruments.



WARNING. Do not remove the safety ground screw from the logic analyzer. The safety ground screw must always be in place to ensure proper grounding of the power supply to the logic analyzer.

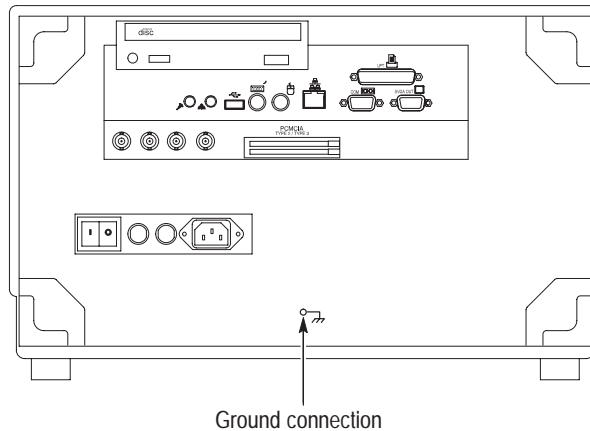
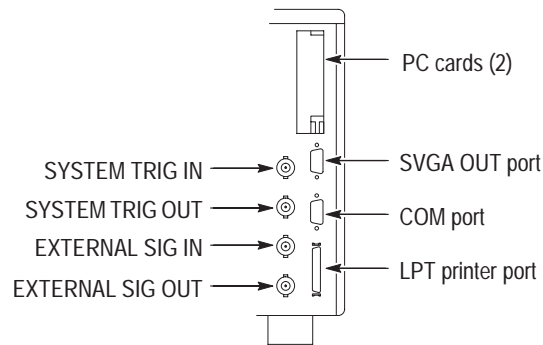


Figure 2–5: Location of ground connection

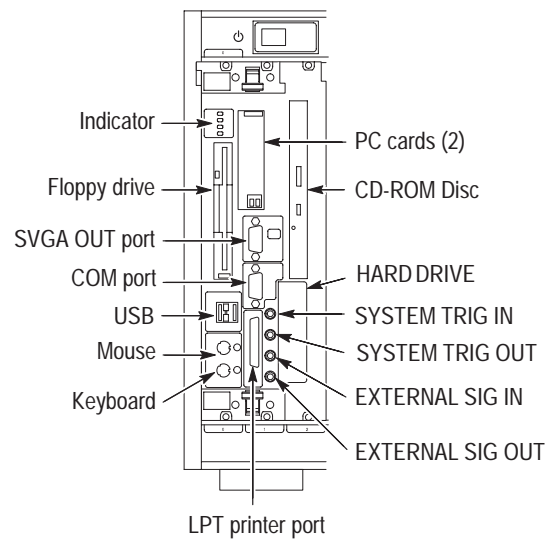
TLA700 Series External Connectors

The mainframe external connectors are shown in Figure 2–6. The following connections are available:

- System Trigger In and System Trigger Out, used to receive or send a trigger from/to an external source.
- External Signal In and External Signal Out, used to receive or send a signal from/to an external source.
- Accessory connections.



Portable mainframe (rear view)



Benchtop mainframe (front view)

Figure 2-6: TLA700 series external connectors

TLA700 Series Chassis Ground Connections

Figure 2-7 shows chassis ground connections. Use the chassis ground connections to connect the grounds of one or more instruments to the mainframe to ensure a common ground connection between instruments.



WARNING. Do not remove the safety ground screw from the benchtop mainframe. The safety ground screw must always be in place to ensure proper grounding of the power supply to the mainframe.

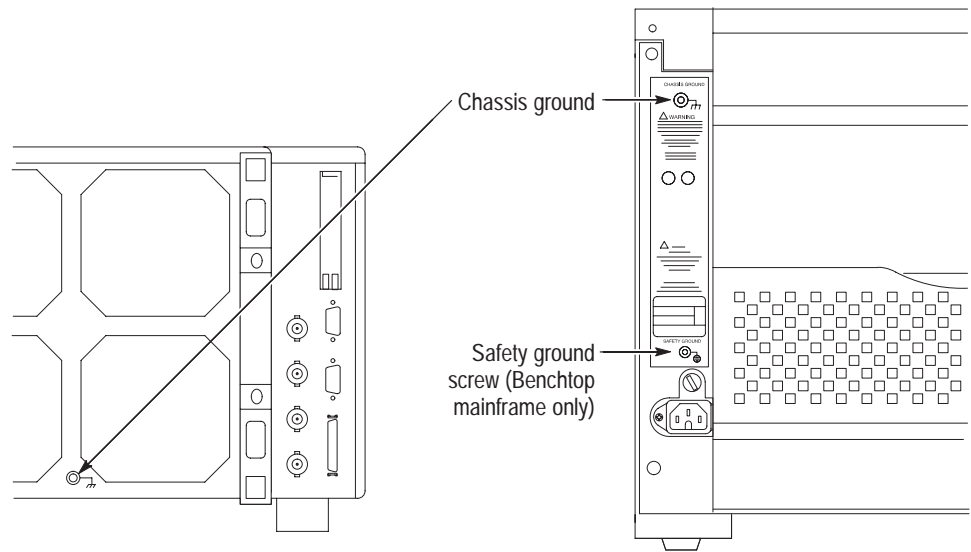


Figure 2-7: Location of ground connections

Approaching the TLA Application Windows

The Tektronix Logic Analyzer application consists of Setup and Data windows as shown in Figure 2–8.

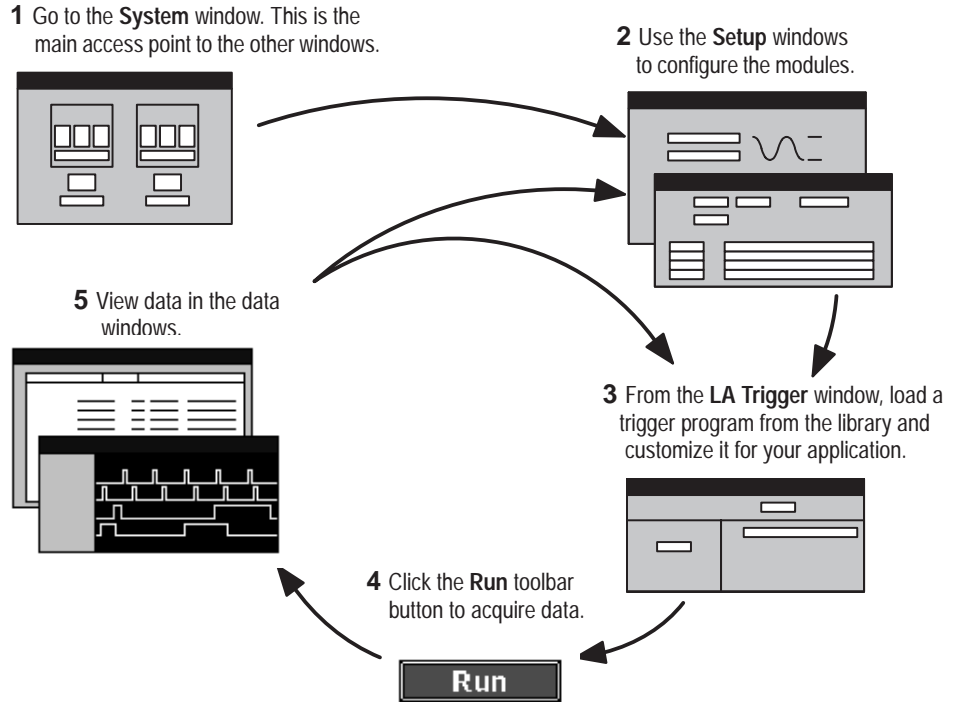


Figure 2–8: Window usage control flow

System Window

The System window is your point-of-entry into the logic analyzer and functions as the overall control center. The System window on a TLA600 series logic analyzer (Figure 2–9) is almost identical to the System window on the TLA700 series logic analyzer (Figure 2–10). The only difference between the two System windows is that the TLA700 series System window reflects the additional modules available with the TLA700 series.

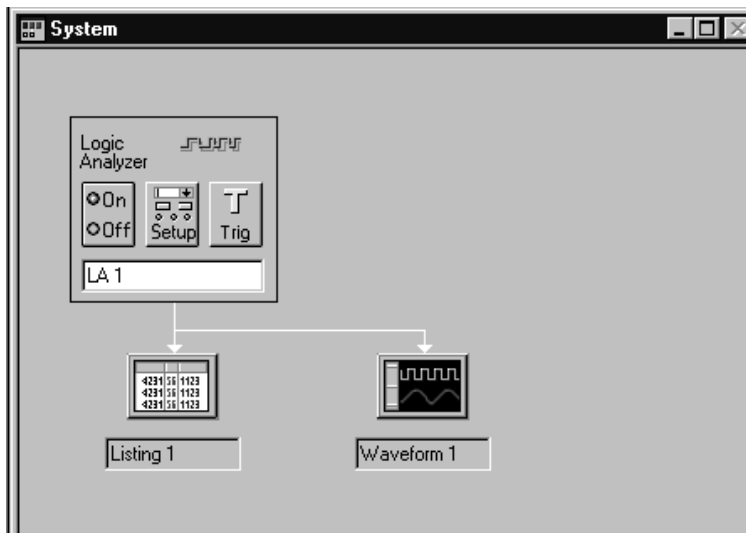


Figure 2-9: System window on a TLA600 series

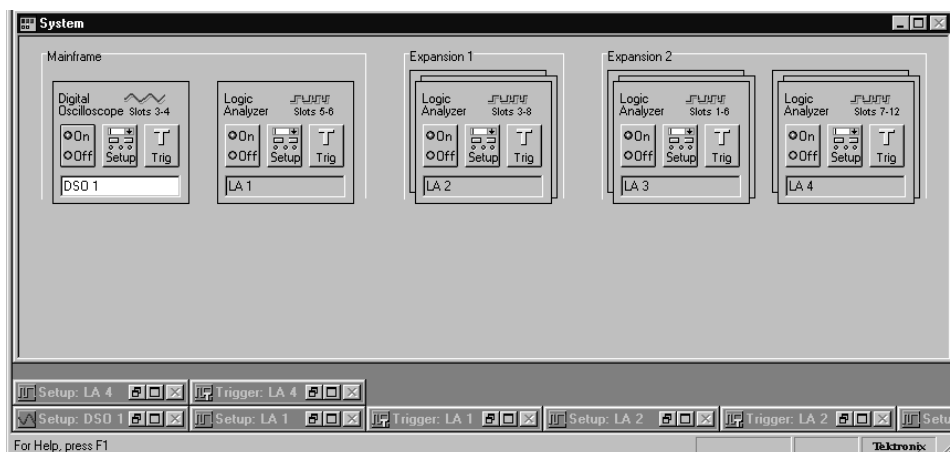


Figure 2-10: System window on a TLA700 series

You can perform the following functions from the System window:

- Open module and data windows by clicking their icons. To select a module without opening its window, click inside the icon.
- Create new data windows through the New Data Window wizard. You can create Histogram windows for performance analysis operations, and Source windows to track the execution of source code. You can also create additional Listing and Waveform windows.

- Use the System window for an overview of how the modules and data windows relate to one another. Relationships between modules (if any) are always shown; to view which modules are associated with a data window, you must select the module icon.
- View which modules provide data to each window by clicking the window name.
- Enable and disable modules by clicking their On/Off buttons.
- Save and load files containing setup, trigger, and data information using the File menu.

Setup Windows

Before you acquire and display data, you must first configure the modules using the module Setup windows. Each module has its own Setup and Trigger window; each module is set up individually. Configure the Setup window before configuring the Trigger window because the Setup window settings affect the Trigger window selections. An example of a logic analyzer Setup window is shown in Figure 2–11.

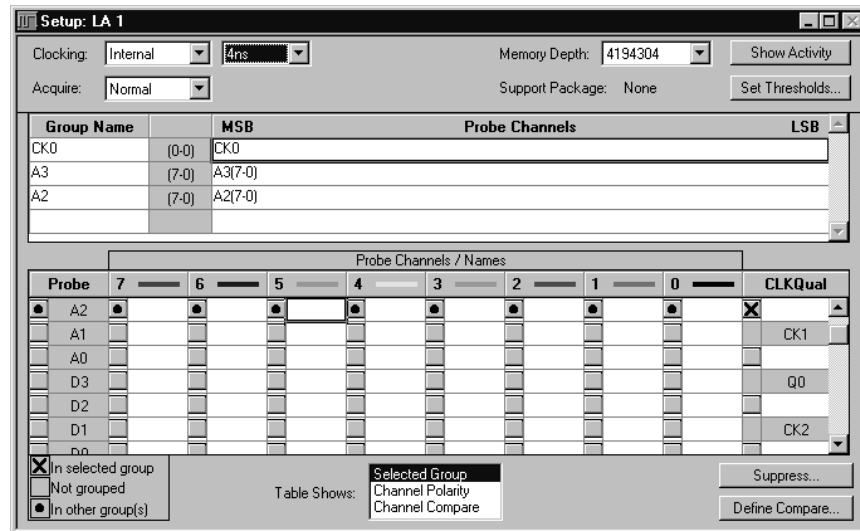


Figure 2–11: LA Setup window

Use the DSO Setup window to define the channel and horizontal setups for the DSO module. An example of a DSO Setup window is shown in Figure 2–12.

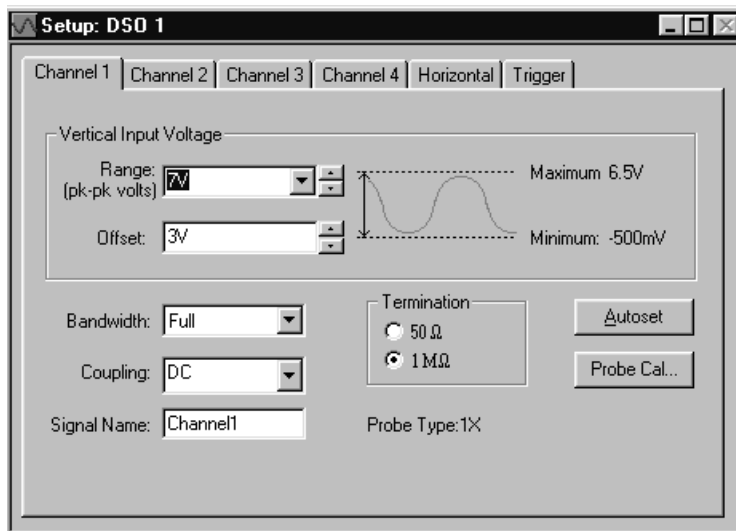


Figure 2–12: DSO Setup window

Trigger Windows

Logic analyzer and DSO modules have their own Trigger windows. Use the Trigger window to define the conditions when the instrument acquires and stores data.

LA Trigger Window

The logic analyzer Trigger window is the heart of the logic analyzer.

A common method for setting up a trigger program is to load a trigger program from the trigger library. With the Trigger window displayed, select Load Trigger from the File menu. Click the Browse Library button to display a list of trigger programs that you can load. You can then alter the trigger program details as necessary.

You can also manually define simple or complex trigger programs one step at a time to determine how the logic analyzer finds the data you are interested in.

See Figure 2–13 for an example of the default LA Trigger window.

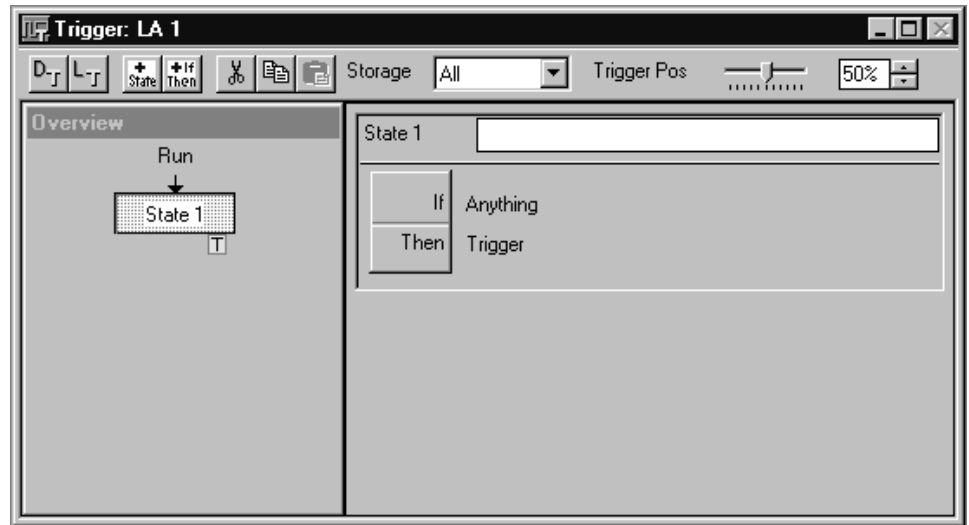


Figure 2-13: LA Trigger window

DSO Trigger Window

The DSO Trigger window lets you define how to trigger the DSO on analog and digital signals. See Figure 2-14.

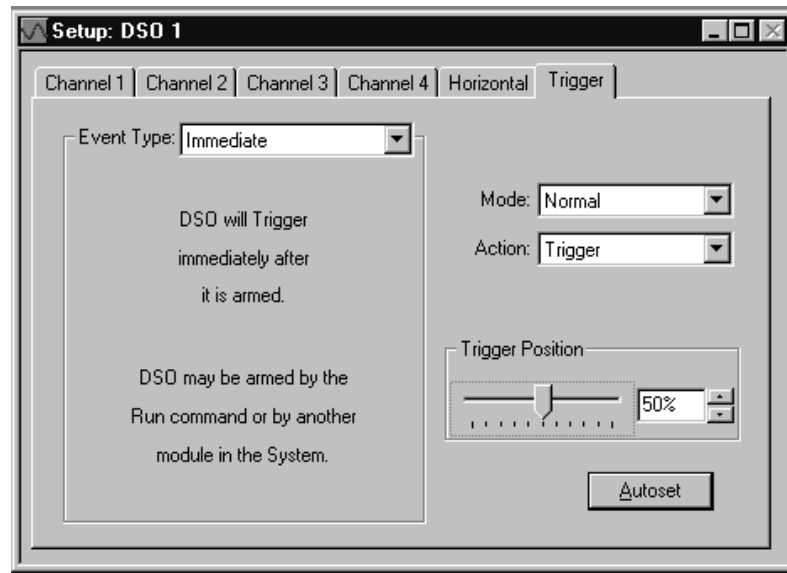


Figure 2-14: DSO Trigger window

Data Windows

You can use data windows to display and analyze acquired data from the logic analyzer or DSO modules. The most common data windows are the Listing windows and Waveform windows. These are the two default windows.

To display and evaluate complex logic analyzer data, you can create other types of data windows using the New Data Window wizard (such as the Histogram window and the Source window). For more information on the New Data Window Wizard, refer to *Creating a New Data Window* beginning on page 3–60 or to the online help.

You can have as many data windows as you want to display different data or different views of the same data.

Listing Windows

Listing windows display logic analyzer data in lists or columns. The following list describes some of the tasks you can perform with Listing windows.

- Place user marks to flag specific data samples for evaluation.
- Use the scroll bars to move through the data or jump to a specific point in the data by clicking the Go To toolbar button and selecting a mark.
- Search for a data event by clicking the Define Search button in the toolbar.
- Add columns by clicking the Add Column toolbar button.
- Move columns by clicking on their labels to select them, and then dragging them to a new location.
- Split the window into two panes for viewing data that is off screen.
- Click and drag columns.
- Identify sample suppression.

Waveform Windows

Waveform windows display DSO or LA waveform data. The following list describes some of the tasks you can perform with Waveform windows.

- Use the cursors to take time or voltage measurements.
- Place user marks to flag specific data samples for evaluation.
- Identify sample suppression.
- View collections of logic analyzer module waveforms as busforms.
- View the value of a logic analyzer module waveform group versus time using magnitude mode.
- Expand and contract busforms.

- Move waveforms by clicking on their labels to select them and then dragging them to a new location.
- Click and drag waveforms.
- Split the window into two panes for viewing data that is off screen.
- Use the scroll bars to move through the data or jump to a specific point in the data by clicking the Go To toolbar button and selecting a mark.

Histogram Windows

Histogram windows display logic analyzer data as histograms. You use Histogram windows to evaluate the performance of software, and is also known as performance analysis. The following list describes some of the tasks you can perform with Histogram windows.

- Use the scroll bars to move through the data.
- Sort histogram data by ranges, counts, or percentages.
- Change the magnification of histogram bars to view the data in greater detail.
- Split the window into two panes for viewing data that is off screen.
- View various statistics on the acquired data.

Source Windows

Source windows display source data. You can track the execution of source code based on the data displayed in a Listing window. The following list describes some of the tasks you can perform with Source windows.

- Step through source code statements.
- Turn source code line numbers on or off.
- Place user marks to flag specific data samples for evaluation.
- Use the scroll bars to move through the data, or jump to a specific point in the data by clicking the Go To toolbar button and selecting a mark.
- Search for source code statements by clicking the Define Search button in the toolbar.
- Determine whether there is any acquired data for the corresponding source file displayed in the Source window.

MagniVu Data

The logic analyzer modules have MagniVu data acquisition as a standard feature. MagniVu acquisition offers 500 ps, high-resolution timing simultaneous with either 100 MHz or 200 MHz state on all channels through the same probes with no double-probing required.

The example shown in Figure 2–15 shows regular data and MagniVu data for the same channels. The MagniVu channels have the “Mag_” prefix with each channel and group names. You can add MagniVu data with the Add Waveform toolbar button.

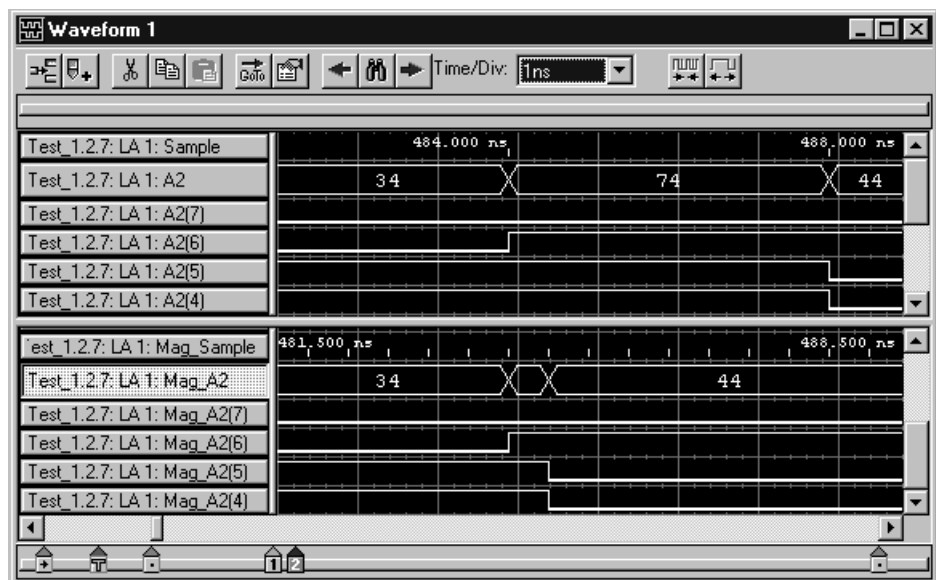


Figure 2–15: Comparing regular and MagniVu data

Saving and Loading Setups and Data

Once you set up the logic analyzer to your satisfaction you will probably want to save the setup for future use. You can save setup information as a saved system file, or as a saved module file.

Saved system files contain setup and trigger information for each module as well as system level information (such as repetitive properties) and data windows for the logic analyzer. Saved module files contain setup and trigger information for only the module specified. In both cases you have the option of saving acquired data with the files.

Execute Save and Load operations from the File menu. For module Save or Load operations, you must first go to the module Setup or Trigger window.

Save the setups and data in a folder where you can easily retrieve them. For example, you may want to save the data in the My Documents folder or within a folder of your own choosing. You should not save the data in a location that may be difficult to find or in a location (such as the Windows System folder) that may cause problems with your operating system.

Avoid using file name extensions other than the default extensions supplied by the system. The logic analyzer may not recognize saved setups with nonstandard file name extensions.

Saved system and module files both contain trigger program information. When you load a trigger from the LA Trigger window, you can select a saved system or module file as the source. When you do so, the logic analyzer extracts only the trigger information from the file and loads it to the module.

Customizing the Display

You can customize your data windows. Using property sheets, you can control data window display parameters. Many screen elements, such as waveforms, columns, and marks, have their own property sheets. Figure 2–16 shows an example of a typical property sheet.

Open data window property sheets by clicking the Properties toolbar button on the data window. Open screen element property sheets by double-clicking on the element or its label.

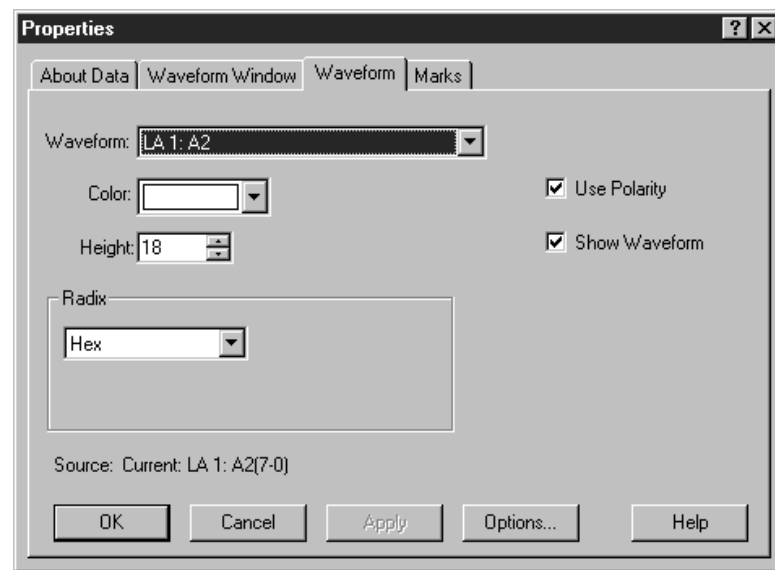


Figure 2–16: Using a property sheet to customize the display

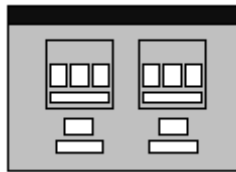
Programmatic Control

In addition to controlling the logic analyzer from the user interface, you can use the TLA700 Programmatic Interface (TPI) to control the logic analyzer from a separate program running on the logic analyzer or on a remote host. Information for using TPI is included as part of the TLA700 online help. A printable version (PDF file) of the TPI online help is available on the instrument. Select Start > Programs > Tektronix Logic Analyzer > TLA Documentation > TPI Manual.

Approaching the Pattern Generator Application Windows

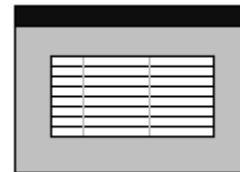
The TLA pattern generator application is similar to the logic analyzer application. Typically you use the windows in the pattern generator application as shown in Figure 2–17.

- 1 Go to the System window. This is the main access point to the other windows.



Press the Program button

- 3 Use the Program window to generate the Block, Sequence, Sub Sequence and Event



Press the Setup button

- 2 Use the Setup window to configure the module



From Block Page

- 4 Use the Listing or Waveform window to generate the pattern data for each block



- 5 Click the Run toolbar button to send the program to the hardware



1. Run the software and click Run on the toolbar to acquire the data

6

2. View the pattern generated in Listing and Waveform windows

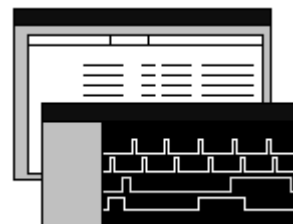


Figure 2–17: Window usage control flow

System Window

The pattern generator System window (see Figure 2–18) graphically represents the pattern generator configuration. The modules are placed in slot order by the application. This window functions as the main application window and provides a familiar starting point for Tektronix logic analyzer users.

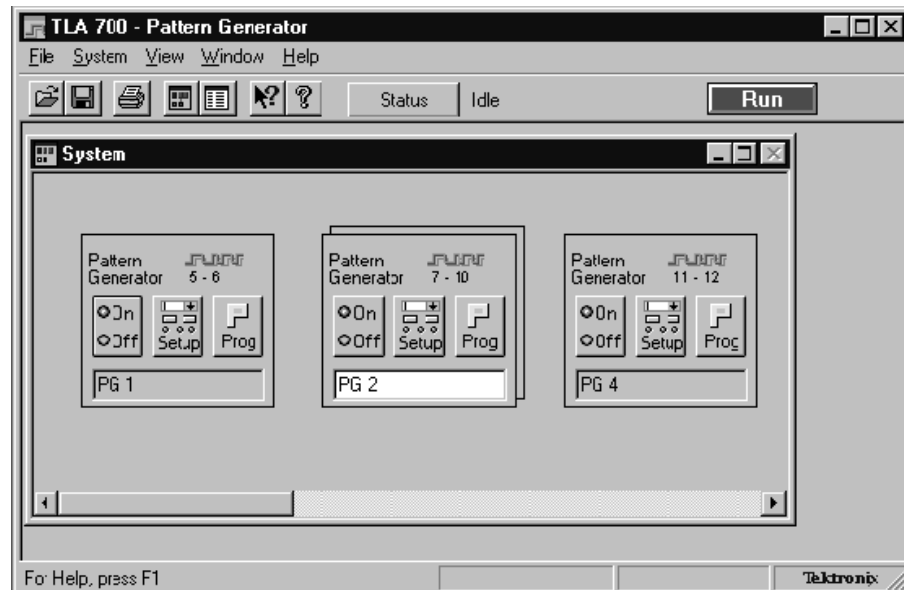


Figure 2–18: System window

You can perform the following tasks in the System window:

- Enable and disable modules by clicking their On/Off buttons.
- Open Setup and Pattern windows by clicking the module icons. To select a module without opening its window, click inside the icon.
- Save and load files containing setup and pattern information from the File menu.

Setup Windows

Before you can generate data, you must first configure the modules using the module Setup windows. Each pattern generator module has its own set of Setup windows. Click on the Setup icon to open the Module Setup window and then select the individual setup windows from tabs at the top of the windows.

Module Setup Window

Use the Module Setup window to set various parameters pertaining to the current pattern generator module such as clocking and the run modes. Figure 2–19 shows an example of the Module Setup window.

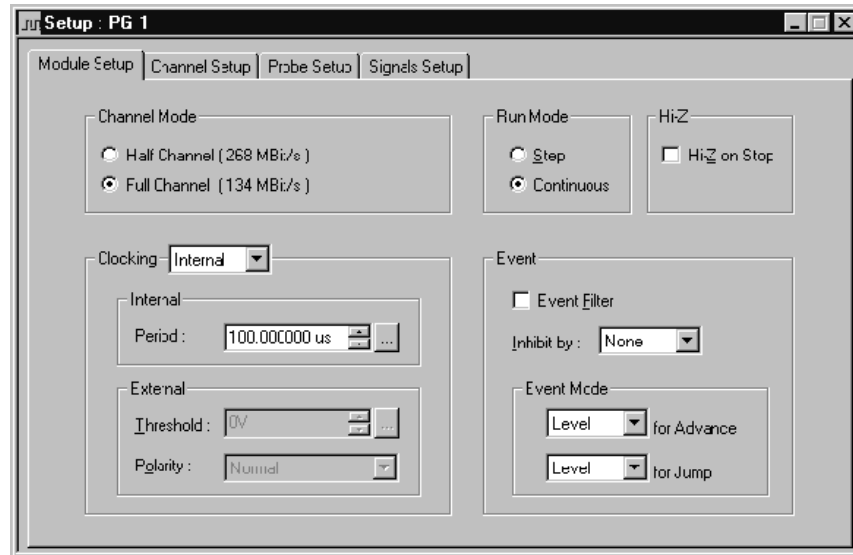


Figure 2–19: Module Setup window

Channel Setup Window

Select the Channel Setup window to define the individual channel setups. The Channel Setup window is similar to the LA Setup window. It shows all of the probe and channel groupings. You can edit the groups as necessary to fit the needs of your application.

Probe Setup Window

Select the Probe Setup window to specify probe details such as the output threshold voltage and inhibit information. The Probe Setup window shows the detailed settings of all probes connected to the pattern generator module.

Signal Setup Window

Use the Signal Setup window to define the input and output signals. Use these signals together with the Program window settings to control the pattern generator program.

Program Window

Use the Program window to develop the pattern generator program. The Program window provides access to the Block Definition window, Sequence Definition window, Sub-Sequence Definition window, and the Event Definition window. Use the Program windows to create the data vectors and the pattern generator program flow.

Block Definition Window

Use the Block Definition window to create blocks of data vectors. The Block Definition window lets you view all of the data blocks in a single window without having to view the individual data vectors. You can assign meaningful names to each data block and then use those data blocks in the Sequence Definition window to create the pattern generator program.

Use the pattern generator Listing and Waveform windows from the Block Definition window to create the data vectors that you want to send to the target system. Figure 2–20 shows an example of the Block Definition window.

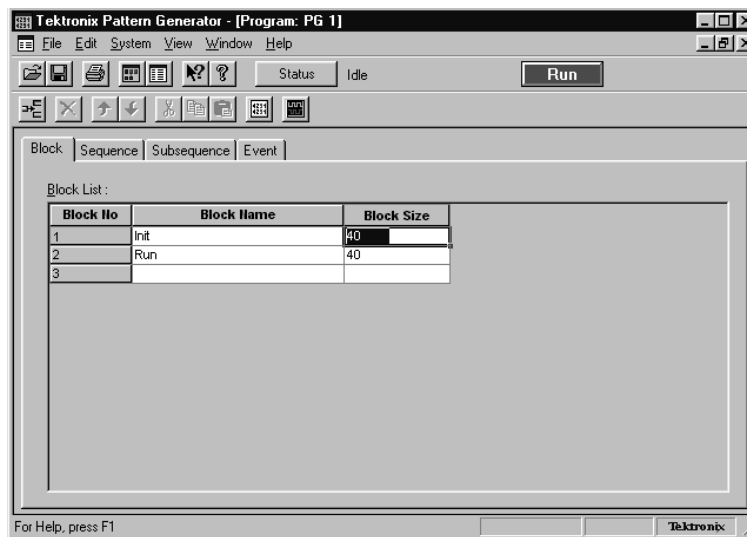


Figure 2–20: Block Definition window

Sequence Definition Window

Use the Sequence Definition window to provide a high-level view of the pattern generator program. Use the data blocks that you created in the Block Definition window together with subsequences, signals, and events to create the pattern generator program. Use labels with each sequence to help control the flow of the pattern generator program.

Subsequence Definition Window

Use the Subsequence Definition window to create subsequences or macros that contain tasks that you may not want visible as part of the high-level sequence flow. You may want to create a subsequence that repeats a series of data blocks before returning control to the main program. You can use meaningful names with each subsequence.

Event Definition Window

Use the Event Definition window to define how to use external signals with the pattern generator program. You can logically AND and OR the probe event inputs to provide program control.

Listing Windows

Use the Pattern generator Listing window to edit the vector data. You can open multiple listing windows to easily move selected data from one block to another by copying and pasting the vector data. You can define the radix to help you set up the vector data. For example, Figure 2–21 shows UserGrp3 with binary data as compared to the other user groups which show their data in Hexadecimal.

Vector	UserGrp1 Hex	UserGrp2 Hex	UserGrp3												UserGrp4 Hex	INHB A	STRE A						
1	0000	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AAAA	0	0		
2	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	5555	1	1		
3	0002	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	AAAA	0	0		
4	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	5555	1	1		
5	0004	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	AAAA	0	0		
6	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	5555	1	1	
7	0006	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	AAAA	0	0		
8	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	5555	1	1	
9	0008	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	AAAA	0	0		
10	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	5555	1	1
11	000A	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	AAAA	0	0		
12	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	5555	1	1
13	000C	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	AAAA	0	0	

Figure 2–21: Listing window

Waveform Window

Use the Pattern Generator Waveform window to edit the vector data. This method may be useful when you want to see the timing relationship between the pattern generator channels. Figure 2–22 shows an example of a Waveform window.

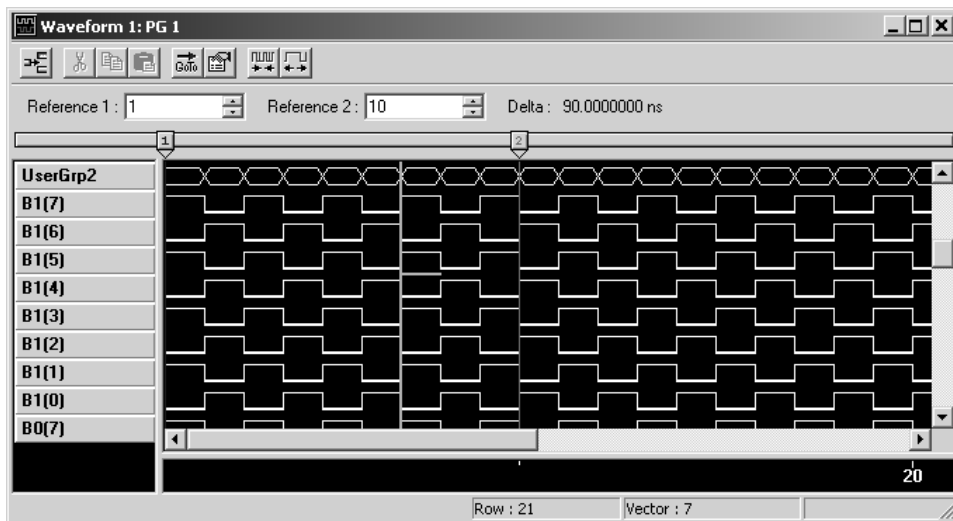


Figure 2–22: Waveform Window

PG Run Properties Dialog Box

The Pattern Generator (PG) Run Properties dialog box selections determine if the logic analyzer Run button will start and stop the pattern generator (PG) modules. Access the dialog box by selecting PG Run Properties from the System menu under the TLA application See Figure 2–23.

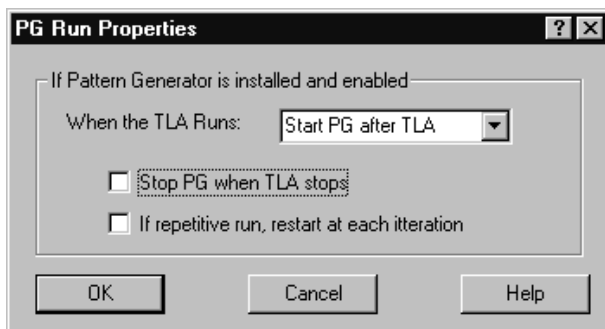


Figure 2–23: Pattern Generator Run Properties dialog box

Operating Basics

This section provides an overview of logic analyzer concepts and some of the features of the Tektronix Logic Analyzer.

To acquire and display signals from the target system, the logic analyzer must perform a complex series of actions. For the most part, these actions are transparent. However, it can be helpful to understand how the logic analyzer operates. This knowledge can influence how you approach a logic analysis problem.

Sampling and Digitizing a Signal

Acquisition is the process of sampling the input signal, digitizing it to convert it into digital data, and assembling it into a waveform record. The order and method of accomplishing these functions is different between the LA and DSO modules.

The LA module converts incoming data into ones and zeros using a comparator with a user-selectable threshold voltage. If the incoming signal is above the threshold voltage, it is converted to a one; if it is below the threshold voltage, it is converted to a zero. After digitizing the data, the LA module samples it at regular time intervals. The sampled and digitized points are stored in memory along with corresponding timing information. (See Figure 2–24.)

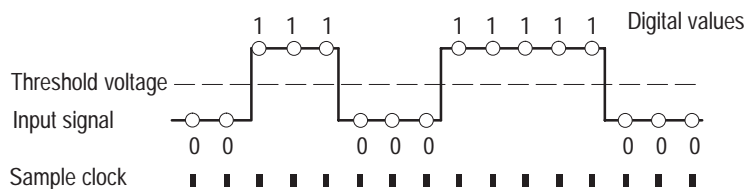


Figure 2–24: Acquiring a digital signal (LA module)

The DSO module samples the voltage level of the signal at regular intervals, and then converts the sampled analog data into 8-bit digital values. (See Figure 2–25.) The sampled and digitized points are stored in memory along with corresponding timing information.

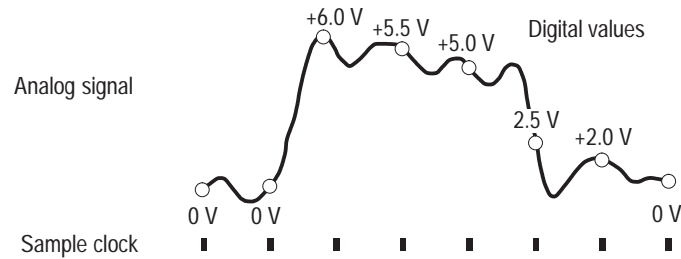


Figure 2–25: Acquiring an analog signal (DSO module)

LA Module Block Diagram

The LA module is the key element of the instrument. Functionally, the LA module can be divided into several blocks, as shown in Figure 2–26. Refer to the figure as you read about the functional blocks.

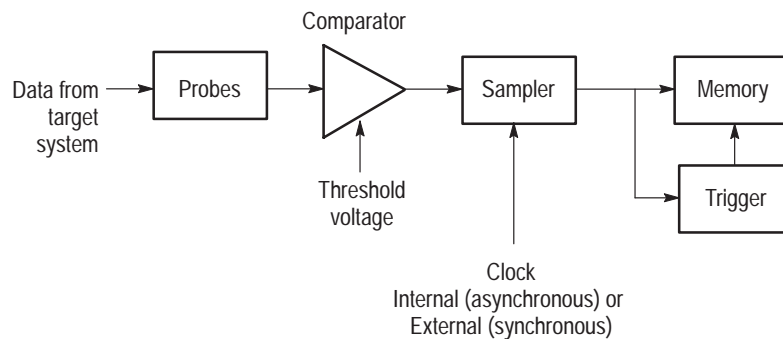


Figure 2–26: Block diagram of the LA module acquisition and storage

Clocking

Clocks control when data is sampled. Naturally, the point at which you sample data has a great deal to do with the type and quality of data you acquire. For the LA module, there are two primary approaches to clocking, external (synchronous) clocking and internal (asynchronous) clocking.

External (Synchronous) Clocking. This clocking mode is called an external or synchronous clock because the clock is external to the logic analyzer, and is synchronized to the target system.

The signal you chose as the external clock to the logic analyzer should be the same signal that controls the activity of the other signals you want to observe. For example, to observe the output states of a counter chip, you might use the clock input to the counter chip to act as the external clock source to the logic analyzer. With this setup, each clock pulse to the counter chip can also be used to clock data from the counter's output lines into the logic analyzer. As another example, to record the data being written to a latch, you could use the load signal to the latch as the external clock source to the logic analyzer.

Internal (Asynchronous) Clocking. Much activity can occur in the target system between system clock signals. Using the LA module's internal (asynchronous) clock, you can view all activity in the target system, not just the data available at the target system clock signal.

Internal clocking is the best choice when you are primarily interested in the timing aspects of the data. Internal clocking is a natural choice for waveform timing analysis. It is important to note, however, that the value of internal clocking is not limited to just displaying waveforms. For a detailed picture of data activity both during and between state changes, use internal clocking. For example, when you use internal clocking you are able to acquire and display glitch information in either the Waveform or Listing windows.

Acquiring Data

When you start an acquisition, the logic analyzer begins sampling data from the probes. Then, each time a sample clock occurs, data is sampled. Sampled data is then sent to the trigger functional block and to the main memory.

Triggering and Storage Qualification

The trigger program looks at sampled data for specific events and then takes a specified action. The trigger program can look for events, such as data values, data ranges, or signals from another module. You can also use internal counters to trigger when the counter reaches a specified value.

When the trigger condition is satisfied, the LA module enables a post trigger delay counter to allow the post trigger portion of the acquisition memory to fill before stopping acquisition.

The trigger function block includes storage qualification that looks at sampled data. If the storage conditions are met, a storage qualifier signal enables sampled data to pass into the acquisition memory as qualified data. Any unqualified data samples are excluded.

Storing Data in Memory

The acquisition memory works like a circular buffer, storing every qualified data sample until the entire memory is full. After that, each new data sample overwrites the oldest existing sample. This process continues until the trigger event is found and the post trigger delay counter reaches the specified value (based on the trigger position selection), which stops acquisition. During acquisition, you can monitor the progress of the data storage process using the Status Monitor.

After storing the data you can display the acquired data in the Listing or Waveform data windows.

DSO Module Block Diagram

The DSO module adds analog analysis capability to the instrument. Functionally, the DSO module can be divided into several blocks, as shown in Figure 2–27. Refer to the figure as you read about the functional blocks.

Probes

A probe interface detects the attenuation factor of each probe. This information is used to set the vertical scale.

Acquiring Data

When you start an acquisition, the DSO module begins sampling data from the probes. Each time a sample clock occurs, data is sampled. Signals from the probes go to the attenuators/preamp functional block, which is responsible for input coupling, termination, bandwidth, offset, and full scale range. The DSO module always uses internal clocking.

From the attenuators/preamp, signals are sent to the acquisition unit and trigger functional blocks.

Acquisition Unit

The acquisition unit functional block samples the input signals and converts them to digital data.

Triggering

The DSO trigger looks at sampled data for a specific event. The trigger can look for various types of events, such as glitches, setup and hold violations, runt pulses, or signals from another module.

When the trigger event is found, the DSO module enables its post trigger delay counter to allow the post trigger portion of the acquisition memory to fill before stopping acquisition. When triggered, the DSO module performs its specified trigger action (for example, triggering all modules).

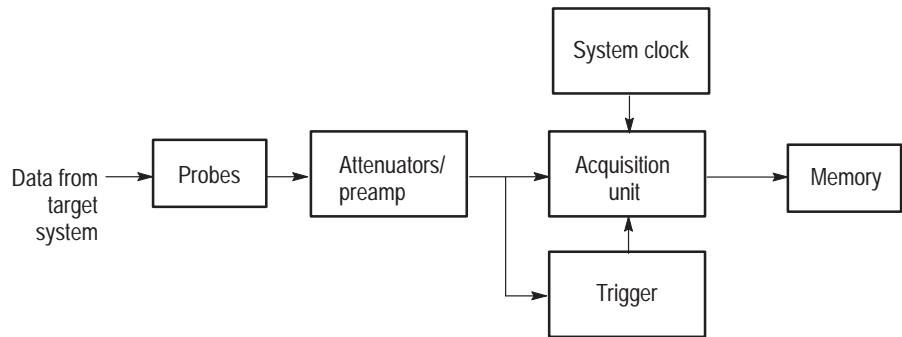


Figure 2–27: Block diagram of the DSO module acquisition and storage

Storing Data in Memory

The acquisition memory works like a circular buffer, storing data samples until the entire memory is full. After that, each new data sample overwrites the oldest existing sample. This process continues until the trigger occurs and the post trigger delay counter reaches the specified value (based on the trigger position selection), which stops acquisition. During acquisition, you can monitor the progress of the data storage process using the Status Monitor.

After storing the data you can display the acquired data in the data windows. In the Waveform window, the data is shown as analog waveforms. In the Listing window, the data is shown as a series of voltage values.

Pattern Generator Module Block Diagram

The pattern generator module adds pattern generator capability to the logic analyzer. You can generate specific data patterns to a target system and then use the logic analyzer to evaluate the resultant data from the target system.

The pattern generator module functionality can be divided into blocks as shown in Figure 2–28. Refer to the figure as you read about the functional blocks.

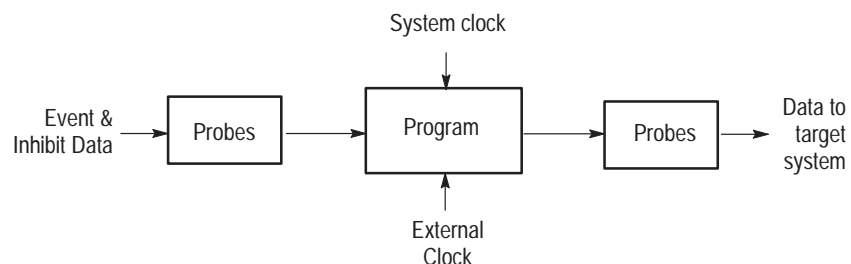


Figure 2–28: Block diagram of the pattern generator module

Probes The probe interface serves two purposes, to detect event and inhibit information and to output data to a target system. In addition to sending pattern generator data to the target system, the probe also sends clock and strobe information.

You can connect up to four probes to a single module. Each probe supports 16 channels in Full-Channel mode and eight channels in Half-Channel mode.

Pattern Generator Program

The pattern generator program is the heart of the pattern generator module. You can create blocks of data vectors to work together to create complex pattern generator programs. The program uses external and internal events to determine specific actions such as loops and branches to other data blocks. The program can be controlled by an internally selected clock or by an external clock through a front-panel BNC connector.

Use the Sequence Definition page of the Program window to set up and define a sequence events that make up the pattern generator program. Each sequence line determines how the pattern generator will use blocks of data that you define in the Pattern Generator Listing or Waveform window. You can set up the program to wait for specific events or signals and then jump to a different sequence when an event is either true or false.

You can also set up the pattern generator to single step through programs and output a single set of vectors with each clock cycle. This is useful for troubleshooting or debugging setups.

Logic Analyzer Physical Model

Physically, the logic analyzer is made up of two main parts: the modules and the mainframe. Figure 2–29 illustrates the relationship between the logic analyzer and its subparts.

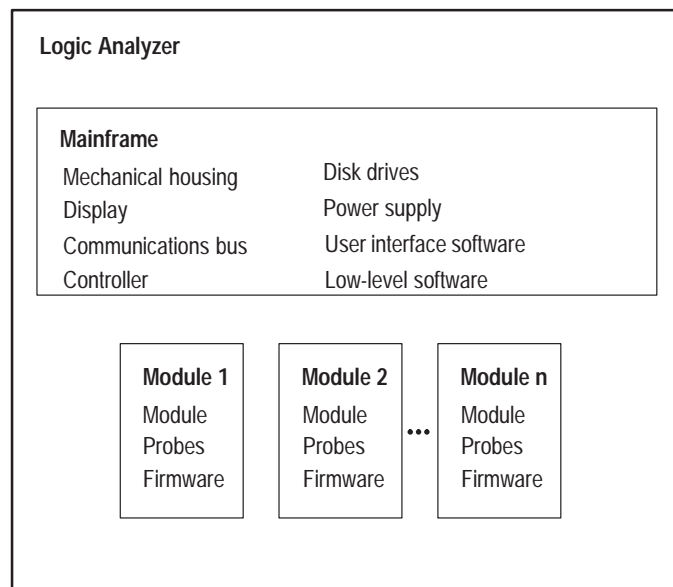


Figure 2–29: Logic analyzer physical model

Logic Analyzer Conceptual Model

Conceptually, the logic analyzer is made up of two main parts: the modules and the system. From the operational perspective, a module encompasses the setup, trigger, and data associated with the physical LA or DSO module installed in the logic analyzer. See Figure 2–30. The system refers to the setup and data for the whole logic analyzer, including all the modules.

Some actions occur at the module level, some at the system level. For example, you can save either module or system files. When you save a module, you save all the setup and trigger information for that module. (You also have the option of saving the data for that module.) When you save a system, you save all the setup information for the system, including data window display settings, and all the module information, as well.

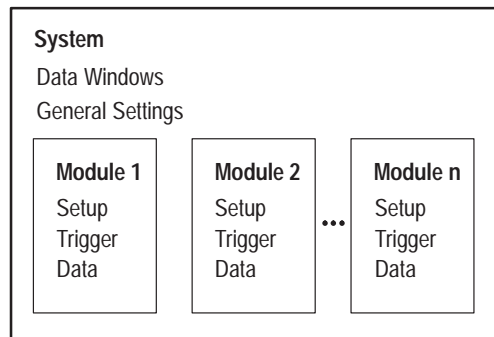


Figure 2–30: Logic analyzer conceptual model

Intermodule Interactions and Time Correlation

Each module has its own setup, trigger, and clocking functions. (LA modules may include microprocessor support as part of their setup.) Each module also acquires and stores its own data.

When you start an acquisition, all modules start acquiring data together. (Exceptions are when one module has been programmed to arm another or when a module has been turned off.) Modules stop acquiring data individually, according to their trigger programming. You also have the option of setting the logic analyzer to operate in repetitive mode, in which the modules acquire data and update the data windows continually until you manually stop the acquisition.

Modules readily communicate with one another by means of their trigger programs. You can specify functions such as the following:

- Trigger all modules (system trigger)
- One module arms another

- Modules respond to events declared by another module (internal signals)

After the modules have captured and stored data, you can view the data in a Listing or Waveform window. All data is time-correlated in the display, regardless of its source. Due to the precise time stamp information stored with the data, and the tightly-integrated communications between modules, the logic analyzer interleaves data acquired from various sources. Because time stamp information is always stored with the data, you can also compare saved data and current data with no loss of accuracy.

MagniVu data is also time-correlated with regular data. Because MagniVu data is always present, you can easily compare a normal acquisition with the MagniVu counterpart.

Listing-Data Concepts

In many cases, you will use the logic analyzer to observe the data flow in the target system. The data recorded by the logic analyzer can be displayed in a listing format, as shown in Figure 2–31.

Listing data is a table of sequential operations performed by the target system. In the Listing window, each data sample is displayed sequentially. Because each data sample includes time stamp information, it is a straightforward process to display acquisitions from multiple data sources. Samples from all specified data sources are interleaved in chronological order. For clarity, each line in the table represents a single data sample from a single data source.

You control the presentation of the data by selecting the display radix of the columns. You can also make other format selections such as font size, color, and column width.

Timestamp	Address	Data	Control	Misc
-562.500 ns	FF607D2A	0000	8FC7	1C
-187.500 ns	FF607D2C	7000	8FC5	1C
0 ps	FF540000	5555	8FCF	1E
375.000 ns	FF607D2E	3007	8FC4	1C
750.000 ns	FF607D30	2F00	8FC7	1C
1.125.000 us	FF607D32	4EB9	8FC7	1C
1.500.000 us	FF006212	0000	AF9F	1E
1.875.000 us	FF006214	5555	AF9F	1E
2.250.000 us	FF607D34	0060	8FC7	1C
2.625.000 us	FF607D36	41AA	8FC7	1C
3.000.000 us	FF607D38	2E1F	8FC5	1C
3.375.000 us	FF00620E	0060	AF9F	1E

Figure 2-31: Listing data

You can include data acquired by the DSO module in the Listing window. The Listing window in Figure 2-32 shows DSO module Channel 1 data as discrete voltage levels. As with any module, the data samples from the DSO module are time-correlated with the other data and appear on separate lines.

Sample	LA CK0	LA A3	LA A2	Timestamp	DSO 1 Channel1
DSO 1	503			-8.342 ns	-50.24mV
DSO 1	504			-7.342 ns	23.87mV
DSO 1	505			-6.342 ns	193.4mV
LA 1	913	0	FF 00	-5.690 ns	
DSO 1	506			-5.342 ns	150.2mV
DSO 1	507			-4.342 ns	163.2mV
DSO 1	508			-3.342 ns	135.2mV
DSO 1	509			-2.342 ns	41.78mV
LA 1	914	0	FF 00	-1.690 ns	
DSO 1	510			-1.342 ns	101.6mV
DSO 1	511			-.342 ps	749.3mV
DSO 1	512			.658 ps	2.648V
DSO 1	513			1.658 ns	3.720V
LA 1	915	0	FF 00	2.310 ns	
DSO 1	514			2.658 ns	4.115V
DSO 1	515			3.658 ns	3.169V
DSO 1	516			4.658 ns	368.7mV
DSO 1	517			5.658 ns	-555.4mV
LA 1	916	0	FF 00	6.310 ns	
DSO 1	518			6.658 ns	-500.4mV
DSO 1	519			7.658 ns	375.8mV

Figure 2-32: Listing window with analog data

Microprocessor Support

For microprocessor applications, the acquired data can be disassembled back into the assembly language mnemonics used by a particular microprocessor. Figure 2–33 shows an example of the disassembled mnemonic display format. Microprocessor support usually requires a special input probe dedicated to a specific microprocessor.

Sample	CPU32 Address	CPU32 Data	CPU32 Mnemonic	Timestamp
0	0000130C	0000	(READ)	(S) -37.529,000 us
1	0000130E	0005	(READ)	(S) -37.154,000 us
2	0060431E	5380	SUBQ.L #1,D0	(S) -36.779,000 us
3	00604320	4A80	TST.L D0	(S) -36.404,000 us
4	00604322	6EEE	BGT.B 00604312	(S) -36.029,000 us
5	00604324	5381	(FLUSH)	(S) -35.654,500 us
6	00604312	0CB9	CMP.L #00000007,0000130C	(S) -35.279,500 us
7	00604314	0000	(EXTENSION)	(S) -34.904,000 us
8	00604316	0007	(EXTENSION)	(S) -34.529,000 us
9	00604318	0000	(EXTENSION)	(S) -34.154,500 us
10	0060431A	130C	(EXTENSION)	(S) -33.779,500 us

Figure 2–33: Listing data using a microprocessor support package

The logic analyzer provides support for a wide variety of different microprocessors. Microprocessor support packages include the software, probe adapters, and documentation.

High-Level Language (Source Code) Support

You can correlate the high-level language (HLL) source code that you wrote with your code as it was executed on your target system and acquired by the logic analyzer. The correlation is based on symbolic information that is extracted from your object file or load module. You configure the logic analyzer to access your source files.

You can step through each executed source statement in the Source window and view the results in a correlated Listing window. You can also set user-defined marks as break points within the code and then trace the execution of the code between the marks. Figure 2–34 shows an example of viewing source code in a Source window, while Figure 2–35 on page 2–34 shows the actual acquired data in an associated Listing window.

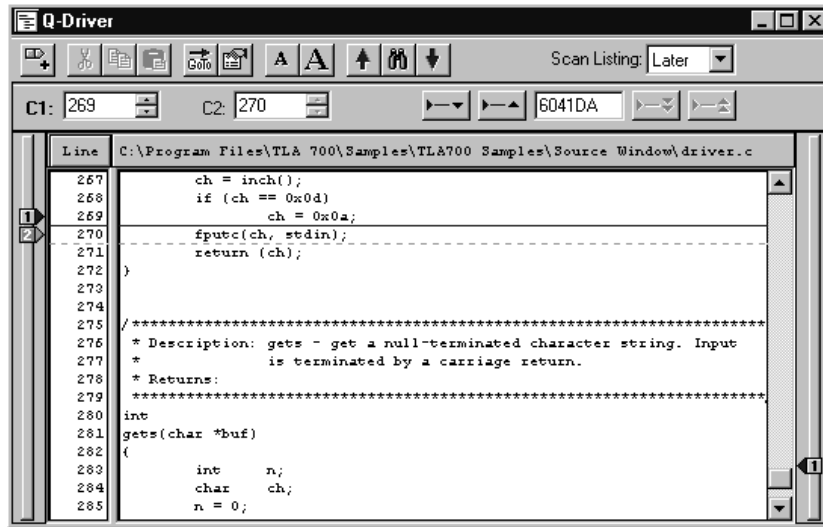


Figure 2-34: High-level source code

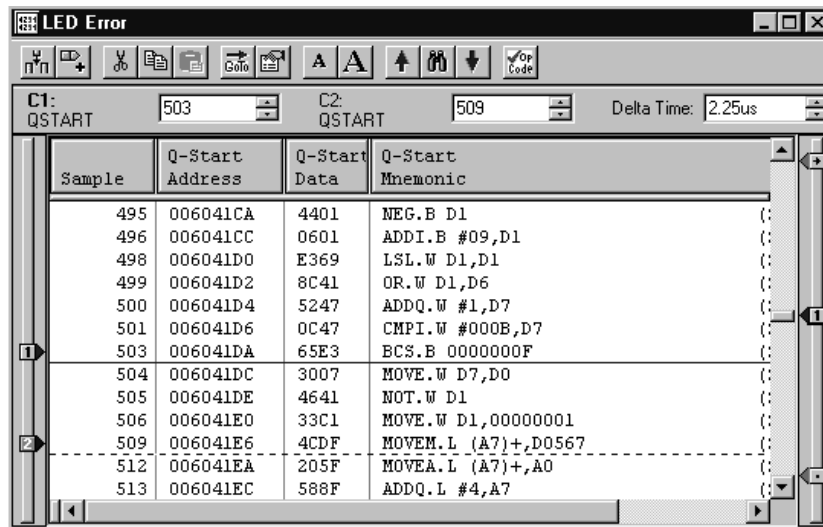


Figure 2-35: Source code viewed as acquired data

The LA module supports a wide variety of object files including IEEE695, OMF51 OMF86, OMF286, OMF386, OMF166, COFF, Elf/Dwarf1 and Dwarf2, Elf/Stabs, and the TLA Symbol File (TSF) format (a text format). Refer to *Appendix B: TLA Symbol File Format*.

Waveform Data Concepts

You can use the logic analyzer to observe the timing relationships between signals by displaying the recorded signal activity as a series of waveforms in the Waveform window. Figure 2–36 shows waveform data from an LA module.

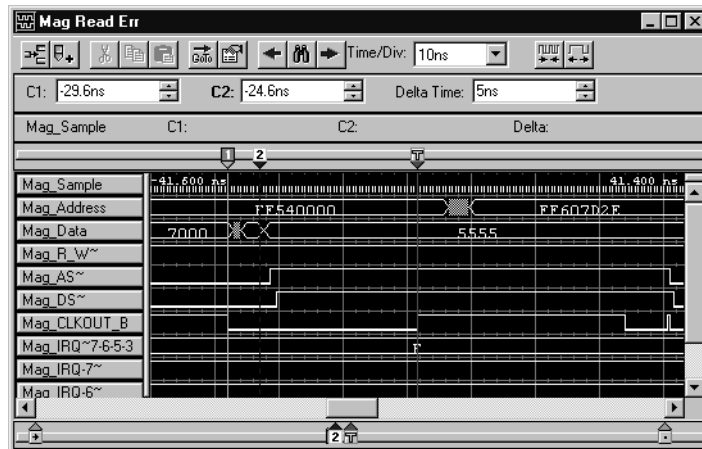


Figure 2–36: Waveform data

Each waveform is displayed in a separate track, but all waveforms are time-aligned horizontally and displayed in the same time per division. Again, the inclusion of time stamp information with the stored data samples makes it a straightforward process to display time-correlated acquisitions from multiple data sources.

You control the horizontal scale of the acquired data in the display. (You do not, however, change setup parameters by changing settings in the waveform display.) You can also make other format selections such as channel group radix, waveform color, and track height. To show when the logic analyzer sampled the data, you can add Sample using the Add Waveform tool bar button.

When viewing LA data, you can view the data as individual channels. You can also display the LA data in groups of channels known as busforms. Use the busforms to display when data changes with respect to clock or control signals.

When you are interested in displaying the value of a group of channels over a period of time, you can use magnitude mode. For example, using magnitude mode, you can view the channels connected to a 16-bit digital counter. The magnitude waveform appears as a sawtooth waveform as the counter values increment from the minimum value (00) to the maximum value (FF).

LA Module Versus DSO Module Waveforms

A logic analyzer waveform appears to have zero-length rise and fall times. This is because the logic analyzer is recreating the waveform from the samples stored in its memory, which are either ones or zeros.

No electronic signal is perfectly digital in nature; there is always some analog component. Consider a fast-rising pulse with ringing on the front edge, or glitches that can occur in a noisy circuit. If you suspect problems caused by analog signal characteristics (such as signal voltages higher or lower than specified voltage levels, or slow transition times), you should use a DSO module to observe the voltage characteristics of the signal. Figure 2–37 shows where the DSO module captured a runt pulse that was below the logic analyzer’s threshold.

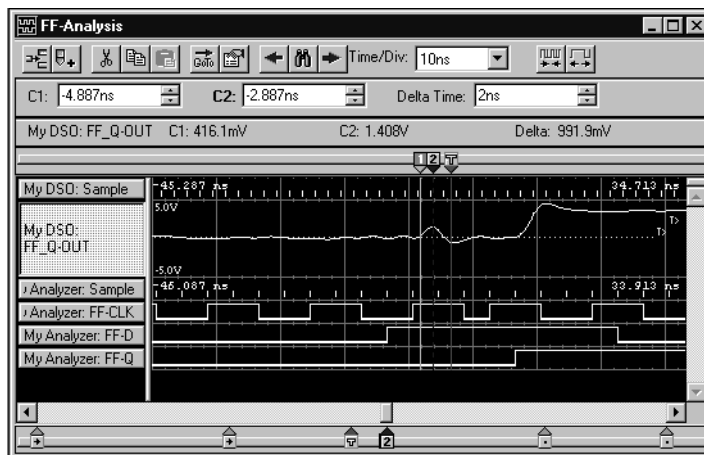
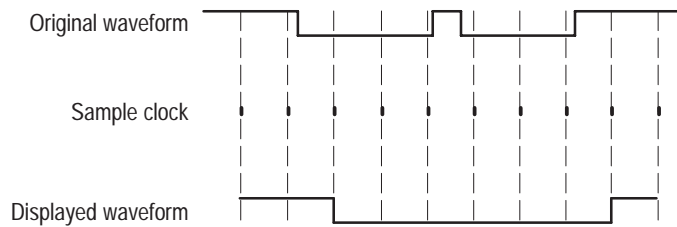
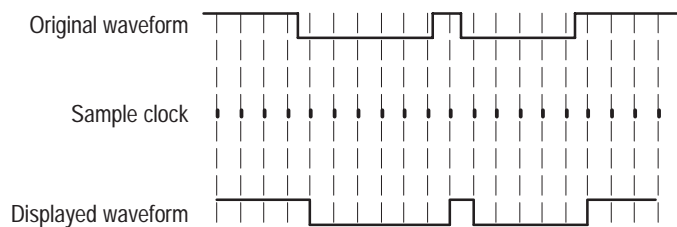


Figure 2–37: Using the DSO module to capture a runt pulse

Sampling Resolution

The accuracy of the waveform recreated from the sampled data depends on the sample clock rate used to record the incoming signals. This is due to the fact that the waveform re-created by the logic analyzer is based on the sampled signals stored in its memory. If the sample clock rate is too low, the recorded data will produce an inaccurate display. Figure 2–38 shows how the sample clock rate can affect an LA module waveform.

Insufficient DSO module sampling resolution can result in aliasing. For information about aliasing, see page 2–38.

Example 1: Slow sample clock**Example 2: Fast sample clock****Figure 2–38: LA module sampling resolution****Signal Resolution and Signal Duration**

There is an important trade-off between the resolution of the recorded signal and its duration in terms of elapsed time. Because the total number of samples that can be recorded by the logic analyzer is fixed by the depth of the logic analyzer's acquisition memory, increasing the sample clock rate provides better signal resolution at the expense of reducing the duration of the captured signal. That is, a faster sample clock rate will record a smaller portion of the signal, but with better resolution; or, you can trade channels or depth to maintain higher resolution.

For the LA module it is important to remember that you have two additional tools to offset the signal resolution/signal duration relationship:

- By using the MagniVu data feature, you can view high-resolution data centered about the LA module trigger. This allows you to zoom in on the data of particular interest while still maintaining visibility of a more extended signal duration.
- By using 2x-Timing mode, you can trade one half the channels for twice the resolution and twice the memory depth. The 2x-Timing is only available with the main timing (not with the MagniVu data feature).

Preventing Aliasing

Under certain conditions, an analog waveform can be aliased on screen. When a waveform aliases, it appears on screen with a frequency lower than the actual waveform being input or it appears unstable. Aliasing occurs because the instrument cannot sample the signal fast enough to construct an accurate waveform record. (See Figure 2–39.)

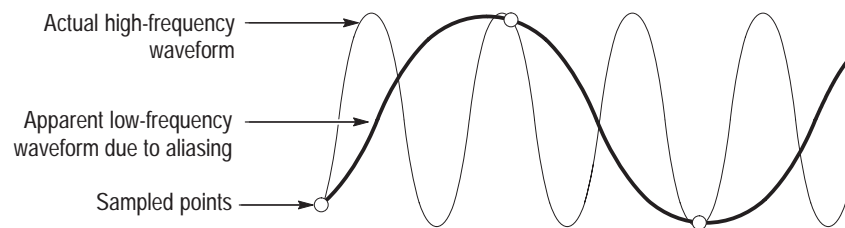


Figure 2–39: Aliasing

To check for aliasing, increase the sampling rate (decrease the clock sample period) in the module Setup window. If the shape of the displayed waveform changes drastically or becomes stable at a faster clock sample period setting, your waveform was probably aliased.

Although the principles of sampling theory define a minimum sample rate of $2X$, a good rule of thumb is to choose a sample clock rate five times faster than the speed of the fastest signal being measured. A faster sample clock rate results in a more accurate reconstructed waveform.

Displaying Waveforms

Waveforms are rarely displayed at an exact one sample point per pixel. Waveforms are usually displayed in a compressed or expanded format. As a general rule, waveforms are compressed when the time per pixel is greater than the time per sample clock. Waveforms are expanded when the time per pixel is less than the time per sample clock.

For compressed DSO module waveforms, the display shows the lowest and highest point that occupy a given pixel column joined by a vertical line. For expanded waveforms, the display points between the actual sample points are calculated.

For expanded DSO module waveforms, *Sin(x)/x interpolation* computes the display points between the actual values acquired.

High-Speed Timing

The LA module provides high-speed timing support through MagniVu data. The MagniVu data is stored in a separate memory that is parallel to the main memory. All data from the sampler goes directly to the MagniVu memory. The MagniVu memory also works like a circular buffer. Unlike the acquisition memory, the MagniVu memory does not qualify data storage through the trigger function block.

MagniVu data is continuously acquired on all channels at the fastest sample rate of 500 ps. Like normal acquisition data, MagniVu data can be displayed in the Listing or Waveform data windows. The MagniVu data is centered on the LA module trigger in the data window. For additional information, see *MagniVu Data* on page 3–72.

Detecting Glitches

One of the logic analyzer's most useful features is its ability to detect and trigger on signal glitches. A glitch is a signal that makes a transition through the threshold voltage two or more times *between* successive sample clocks. Because glitches are often signal transitions that occur intermittently, they can cause circuit malfunctions that are extremely difficult to diagnose.

Although you could try using a very fast sample clock rate to ensure that you never miss any glitches, a better solution is to use the glitch-detection feature. The logic analyzer can trigger on a glitch, either alone or in combination with other signal events. This capability is useful for catching intermittent glitches that might not occur very often, or only when a particular operation is taking place.

You can capture noise spikes and pulse ringing using the glitch capture feature. Figures 2–40 and 2–41 show data captured by triggering on a glitch. In the Waveform window, a glitch captured by an LA module is indicated by a band of color. (See Figure 2–40. For clarity, an arrow identifies the glitch in the figure.)

You must select internal clocking to use the glitch detection feature.

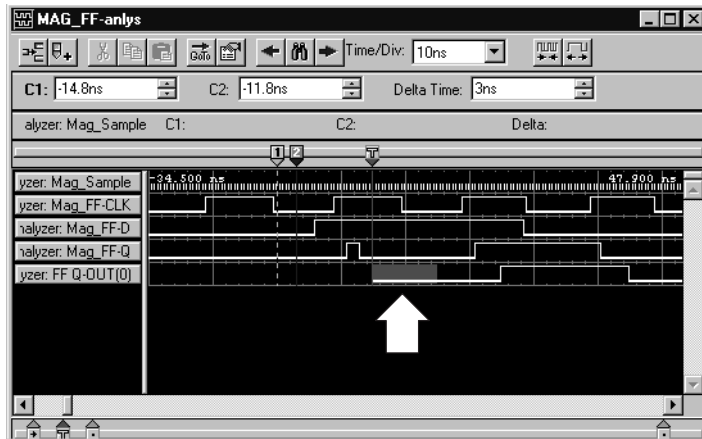


Figure 2-40: LA module triggering on a glitch

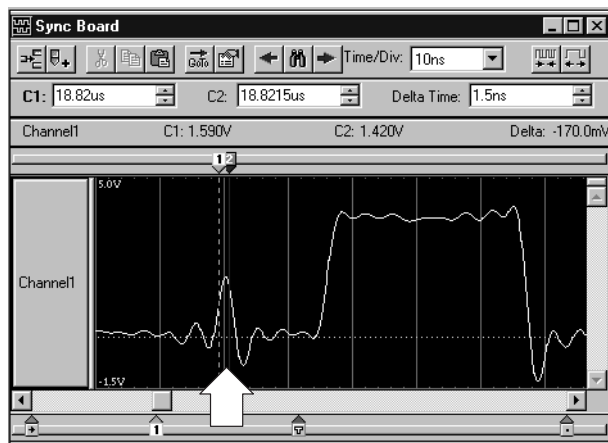


Figure 2-41: DSO module triggering on a glitch

Performance Analysis Concepts

For performance analysis applications, you can use the Histogram window to view the performance of your software. The actual data is displayed as horizontal bars in a histogram.

You may want to use the Histogram window to see which one of your software routines is taking up most of the CPU time. Or, you can use the Histogram window to measure the amount of time used by a particular subroutine. You can use a symbol file to view each of the routines by name.

Figure 2–42 shows an example of the Histogram window where the StopLite routine is taking up most of the computer resources.

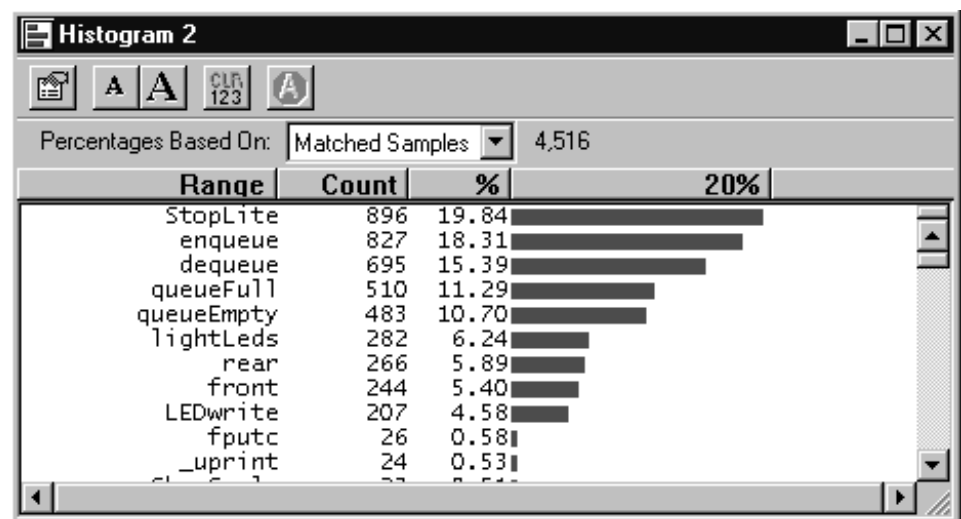


Figure 2–42: Viewing the performance of code with a Histogram window

Comparing Acquired Data Against Saved Data

You can use the LA module to compare acquired data against saved reference data. Use the LA Setup menu to define the data channels that you want to use during the compare operations. You can further define the number of samples that you want to compare as well as data alignment offset.

In the Listing and Waveform windows, you can use color to quickly identify the compared data. You can set up one color to show where the acquired data does not equal the reference data. You can use another color to show where the acquired data equals the reference data.

Figure 2–43 shows a Listing window during a memory compare operation. Notice that some of the data under the LA 2 A2 column appears in a different color, indicating that there were differences between the acquired data and the reference data.

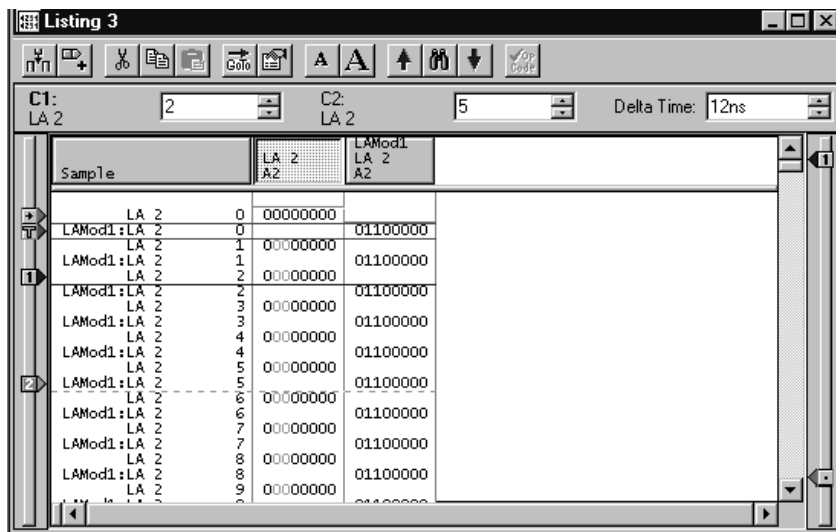


Figure 2–43: Using color to show memory differences in a Listing window

Repetitive Acquisitions

Use the Repetitive acquisition features of the logic analyzer to automate repetitive and time-consuming tasks. For example, you can specify the number of times that you want the logic analyzer to acquire data. With each acquisition, you can save the data to a file for analysis. You can also set up the logic analyzer to open a file or execute a program when all of the acquisitions have been completed.

You can set up the LA module to acquire and compare the acquisition data against known reference data. The LA module can continue acquiring data until there is a mismatch between the acquisition data and the reference data.

Figure 2–44 shows an example of such a setup where the acquired data is exported to a file for each acquisition. When a data-mismatch occurs the logic analyzer stops acquiring data and exports the data to a file. The faulty data can now be analyzed by another application.

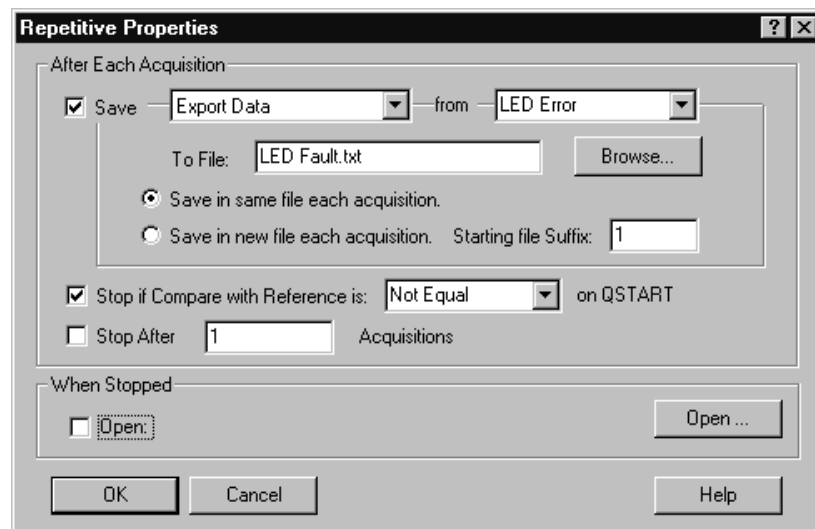


Figure 2–44: Defining repetitive setups

Symbol Support

Symbols simplify tasks, such as setting up triggers or identifying specific values within the data. When you program a trigger or view data, it is cumbersome to remember which numeric channel group values correspond to particular machine instructions or code modules. The logic analyzer makes this task more manageable by allowing you to assign symbolic names or mnemonics to group values.

For example, you might assign the symbol `WRITE` to the control bus event that causes the target system to write to a memory location. Then, if you wanted to trigger when a write cycle occurs, you could enter `WRITE` in the trigger program in place of the actual data value. You could also choose to have `WRITE` appear in the Listing window for quick identification of the instruction.

In Figure 2–45, the example shows a trigger program which uses the symbol `SYSTEM_RESET` as part of the trigger clause.

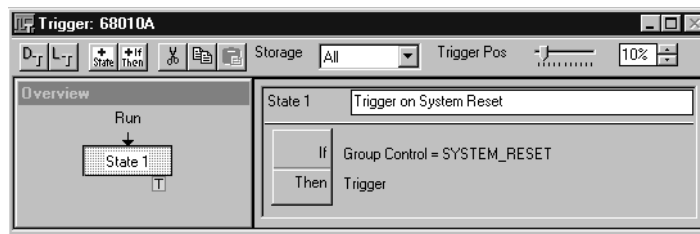


Figure 2–45: Using symbols in a trigger program

You can use symbol files with a Source window and an associated Listing window to track the execution of source code. The symbol file provides the information to associate a line of source code to an address in a Listing window. When you move a cursor in one window, the symbol file provides the necessary information to move the cursor to the correct location in the other window.

Often, the application software will define symbols for you. For example, when you load a microprocessor support package, symbols are also loaded (typically, to the control group). These symbols represent data values that correspond to bus cycle types. Other software applications produce range symbol files which you can load (typically, these files are loaded to the address group).

Symbol Files

To use symbols, you must first load or create one or more symbol files that define the symbols. Symbol files contain symbol names and their associated data values. You can use symbol files created by another application, edit symbol files from other applications, or you can create your own symbol files using a text editor.

Each entry in a symbol file consists of an alphanumeric symbol name with its associated numeric value or range of values. After you create a symbol file, you can specify the symbol file for the appropriate channel group in the Waveform or Listing window, use symbolic names as a substitute for numeric values in the Trigger and data windows, and use symbols for tracing source code in a Source window.

Symbol files perform like look-up tables. For example, if the address of a printer I/O port is at address F734BC, you can define a symbol, printer-port, that corresponds to that value. Then, in the Trigger window, you can specify the symbol name as an event in the trigger program and cause the module to trigger when printer-port (F734BC) appears on the address bus. You can also specify the symbolic display radix for the address channel group and the symbol name printer-port will show in the Listing window every time F734BC appears on the address bus.

Symbol Types. Two main types of symbol files are possible: pattern symbol files and range symbol files. Range symbols can be further divided into three different categories: functions, variables, and source code (source). Table 2–1 shows the different types of symbols and the windows where they are commonly used.

Table 2–1: Using symbols in logic analyzer windows

Window	Pattern symbols	Range symbols		
		Functions	Variables	Source code
Listing	Yes	Yes	Yes	Yes
Waveform	Yes	Yes	Yes	Yes
Histogram	No	Yes	Yes	No
Source	No	No	No	Yes
LA Trigger	Yes	Yes	Yes	Yes

Pattern Symbols. Pattern symbols consist of data patterns up to 32 bits. Each bit in a pattern symbol can be 0, 1, or X (don't care). Pattern symbols are used when a group of signals define a logical state. For example, a microprocessor has a set of pins that indicate the type of bus cycle in progress. A memory read cycle is indicated when the RD \sim and MREQ \sim pins are 0 (logic low) and the BUSAK \sim and M1 \sim pins are 1 (logic high). You can define a pattern symbol name called mem-read that corresponds to bit pattern 1100 and thereby mark all memory read bus cycles in the Listing window. For other bus cycles the logic state of these pins is also important and you can define different bit patterns for each cycle type.

Figure 2–46 shows pattern symbols used in a Waveform window.

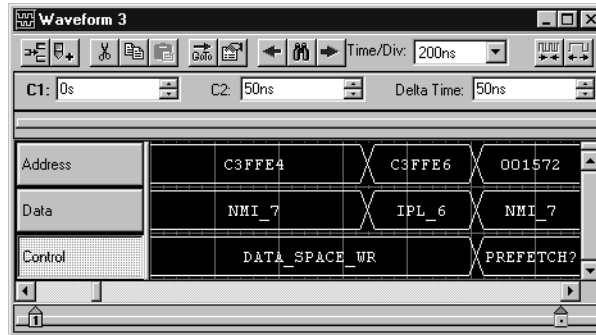


Figure 2–46: Waveforms using pattern symbols

Range Symbols. Range symbols define a range of 32-bit addresses represented by a contiguous set of integers, marked by specific lower and upper bounds. The different types of range symbols are discussed in detail under *TLA Symbol File Format* beginning on page B–1.

When defining a range symbol file, do not overlap ranges of values. If ranges overlap, they may not be recognized. For example, if SYM1 covers the range 1000–3FFF, and SYM2 covers 2000–2FFF, then the values in range 2000–2FFF may be recognized as either SYM1 or SYM2, and the values in the range 3000–3FFF may not be recognized as SYM1 at all.

The range symbols shown in Figure 2–47 define subroutine boundaries.

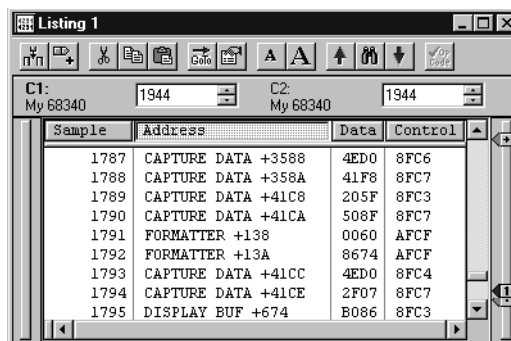


Figure 2–47: Listing data using range symbols

Symbols Dialog Box

Use the Symbols dialog box to provide an overview of all currently loaded symbol files (see Figure 2–48). You can display information on all symbol files currently used by the logic analyzer.

The following status information is available for each currently-loaded symbol file:

- The last time the file was loaded into the logic analyzer application software. It also includes error and warning messages associated with the last load.
- When the file was last modified. The logic analyzer also displays a message if the file may need to be reloaded (such as when the file is modified after it was first loaded).
- The format of the loaded file.
- If the file can be unloaded or if the file is currently in use. Symbol files can only be unloaded if no data windows or setups are using them.

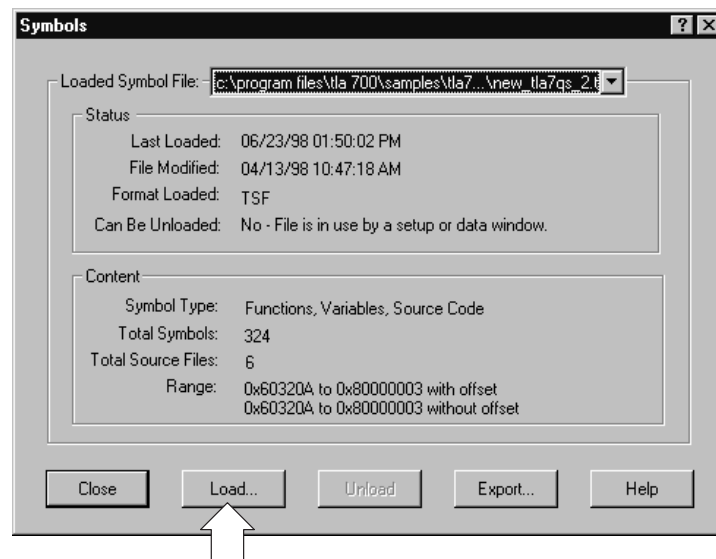


Figure 2–48: Symbols dialog box

The following information is displayed in the Symbols dialog box:

- Whether the file is a pattern symbol file or a range symbol file. If the file is a range file, this field also lists the types of symbols loaded.
- The number of symbols loaded from the file. Symbol files can have an unlimited number of symbols. The number of symbols is limited by the amount of memory. When you load a symbol file, the symbols are placed in memory. Because symbol files consume memory, you should unload unused symbol files to keep memory available for your main application.
- The number of source files referenced by source code symbols loaded from the file.
- The minimum and maximum address values and offset information.

Click the Load button (see Figure 2–48) to open the Select Symbol File dialog box and load a new symbol file. You can browse the file system for the symbol file. If the symbol file is a range file, you can click the Options button in the Select Symbol File dialog box to open the Load Symbols Options dialog box.

Click the Export button to save the current file as a TSF-format symbol file. You can view the exported symbol file with applications such as Wordpad. Edit the symbol file by saving it under a new name and using a text editor. Save the edited file in text format. You can then load the edited symbol file.

Load Symbol Options Dialog Box

Use the Load Symbols Options dialog box (see Figure 2–49) to specify options for range symbol files before loading them into the system.

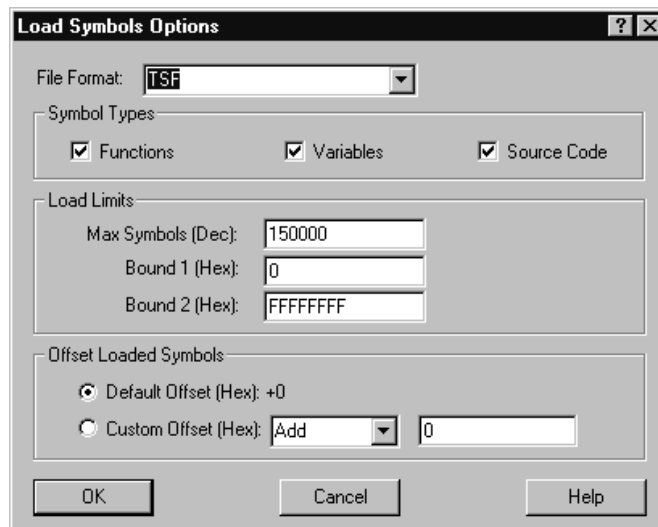


Figure 2–49: Load Symbol Options dialog box

Select one or more of the symbols types to load. If you want to use the symbol file with the Source window, you should be sure to select Source Code symbols.

You can enter a decimal number for the maximum number of symbols to load. The maximum number of symbols that you can load is limited only by the amount of memory available. The file loads symbols until the specified maximum number of symbols is reached. Additional symbols are ignored, even if they fall within the Bound 1 and Bound 2 range limits.

The Bound 1 and Bound 2 fields define the range of symbol addresses that will be loaded. You can enter any hexadecimal values from 0 through FFFFFFFF. Symbols with values outside of these limits are ignored and will not be loaded.

NOTE. *If the lower bound of the range symbol is within the Bound 1 and Bound 2 limits and the higher bound is not, the entire symbol will be valid. However, if the higher bound is within the Bound 1 and Bound 2 limits and the lower bound is not, the entire symbol will be ignored.*

Select either Default Offset or Custom Offset to apply an offset to the symbol values. If you select Default Offset, the default offset is read from the source file and applied to each symbol in the file as it is loaded. If you select Custom Offset, you can add or subtract the specified offset value to each symbol in the file as it is loaded. You can choose any 32-bit hexadecimal value from 0 to FFFFFFFF.

When you enter bound values, enter the values without an offset value. If your application adds an offset, you must subtract the offset value before you enter the bound values.



Reference

Setup

This section describes how to set up the logic analyzer (LA), DSO modules, and pattern generator modules.

For further details, particularly about selections available to you in windows and dialog boxes, please refer to the online help.

Starting From the System Window

The System window gives an overview of the logic analyzer configuration, arming, and triggering relationships. The System window also indicates whether LA modules are merged. See Figure 3–1.

A black arrow from one module to another indicates that one module is set up to arm another. Figure 3–1 shows the merged LA module arming the DSO module.

A module that is programmed to cause a system trigger has an indicator symbol on the right edge of the module graphic.

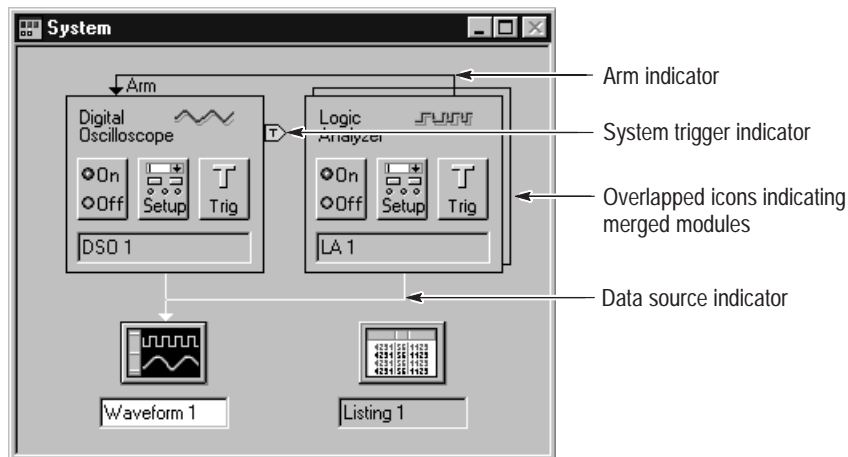


Figure 3–1: System window

Opening Other Windows from the System Window

You can use the System window as a quick navigation tool.

- To open a module Setup, Trigger, or Program window from the System window, click the Setup or Trigger button in the module icon.
- To open a data window from the System window, click the data window button. See Figure 3–2.

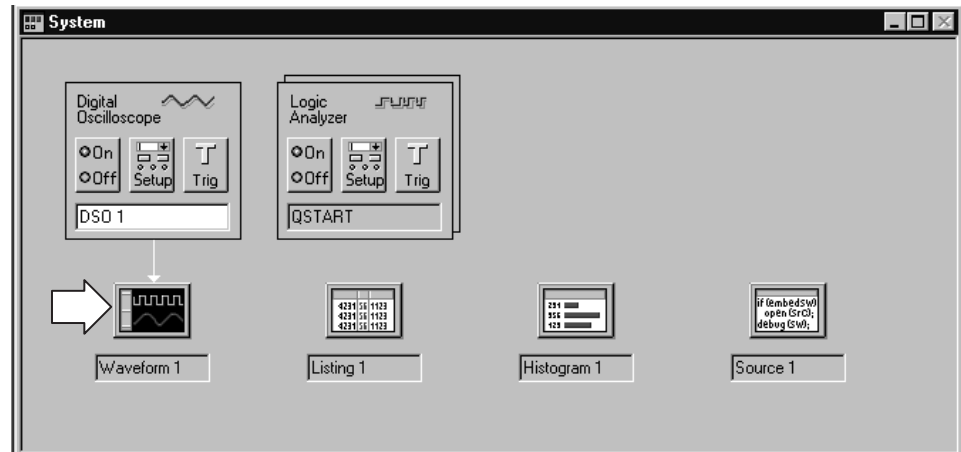


Figure 3–2: Opening a Waveform window from the System window

Disabling Modules

If you are not using a module, you can disable it by clicking the module On/Off button. When you disable a module, make sure that no other trigger programs depend on that module's output.

Renaming Windows

You can rename the windows by selecting the current window labels and overtyping. Names must be unique and are limited to the space available.

Identifying Modules

If you are unsure which physical module is represented by an icon, double-click on the icon to open its System Properties page. This property page lists information about the module, including the mainframe slot numbers in which it is installed. (Slot numbers are indicated on the mainframe.)

Setting Up the LA Module

The primary function of the Setup window (see Figure 3–3) is to configure the LA module for compatibility with the target system. This is where you specify channel groups, set thresholds, and select the sample clock rate. Additional selections configure the LA module for best compatibility with the type of data you want to acquire.

Before you acquire and display data, you must first set up the LA module using the LA Setup and Trigger windows. Together, these windows determine the data to be acquired.

Each module has its own Setup window and Trigger window, each is set up individually. You should configure the Setup window before the Trigger window, because some of the Setup window settings affect Trigger window selections.

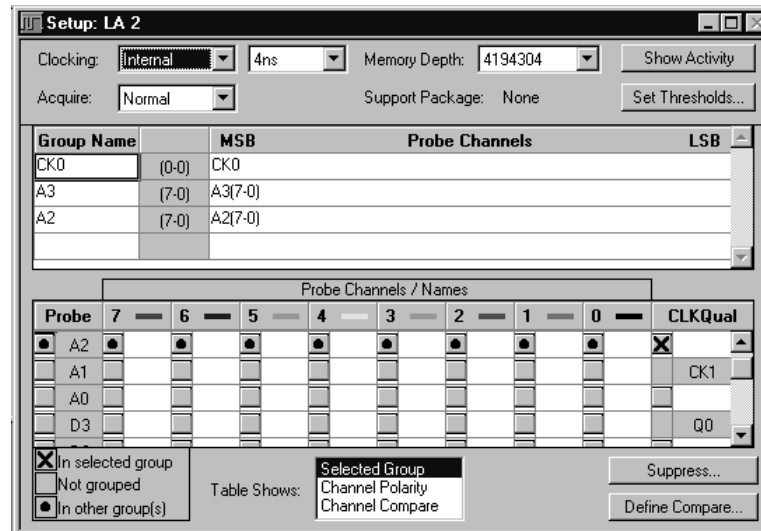


Figure 3–3: The LA module Setup window

NOTE. If you intend to use merged modules, turn to page 3–43 for information before you proceed with the setup procedure.

Microprocessor Support Setup

If you intend to use a microprocessor support package, load it before completing the entries in the Setup window. The microprocessor support package configures the Setup window for you.

To load a microprocessor support package, go to the File menu, click Load Support Package, select the support package you want to load, and then click Load.

After loading the microprocessor support package, the LA Setup window shows the channel definitions, channel groups, and clocking requirements for the microprocessor support package. Figure 3–4 shows an example of the LA Setup window after loading the QSTART support package.

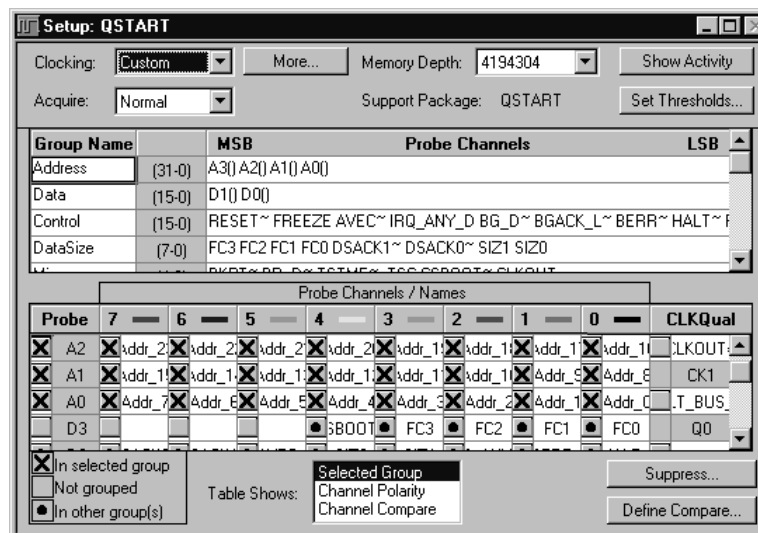


Figure 3–4: Setup window with the QSTART support package

For information about microprocessor support packages, refer to the online help and to the instruction manual that came with your microprocessor support package.

Performance Analysis Setups

If you intend to do performance analysis with your LA module, you may want to load a microprocessor support package which contains the predefined channel setups and clocking setups. You can also define the channel and clocking setups in the Setup window if you are not using a microprocessor support package.

Sample Suppression

You can use sample suppression to suppress or hide samples in the display windows. This can be useful to help you focus on the data that you want to see. When you suppress data samples, the suppressed samples are still in the acquisition memory; you can turn the sample suppression off to view all the data.

Click the Suppress button at the bottom of the Setup window to display the Sample Suppression dialog box (see Figure 3–5). Select one of the options to define the data suppression. You can select a similar dialog box by right-clicking in one of the display windows.

For more information on data suppression, refer to the online help.

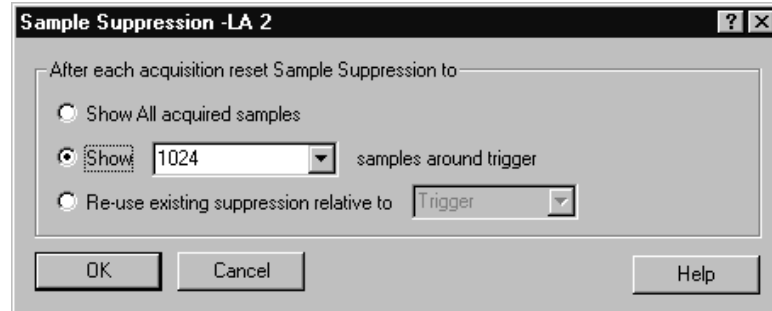


Figure 3–5: Sample Suppression dialog box

Memory Compare

Memory Compare allows you to compare the current acquisition data of an LA module against a known reference data. You can quickly view data differences and similarities in a Listing or Waveform window using user-defined colors.

Selecting Channels for the Memory Compare. Choose the channels that you want to compare in the LA Setup window by selecting Channel Compare in the Table Shows box (see Figure 3–6). You can then compare all data channels, specific channel groups, or individual channels by selecting the appropriate channels in the Probe Channels/Names table.

After selecting the channels that you want to compare, click the Define Compare button in the lower-right corner of the Setup window to define the compare actions.

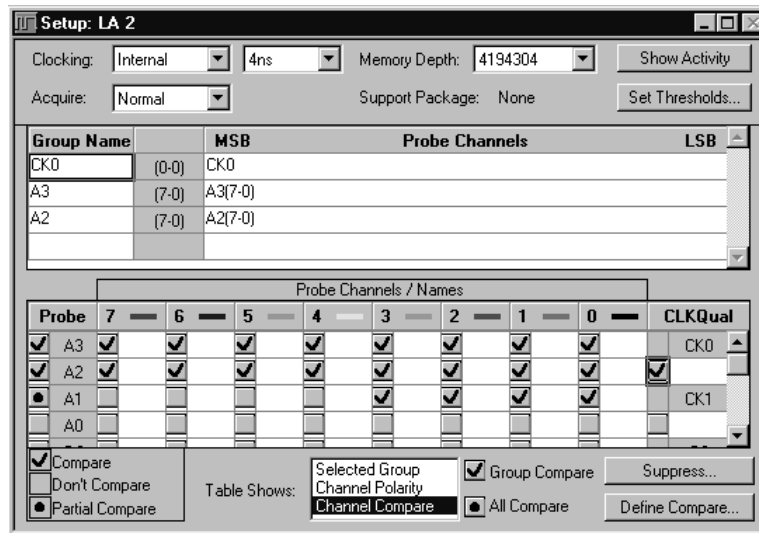


Figure 3–6: Selecting channels for memory compare

Defining Memory Compare Parameters. Select Enable Data Compare in the Compare Definition dialog box as shown in Figure 3–7. Select the reference data source in the box; if the data source that you are interested in does not appear in the list, click Add Data Source to browse for the data source in the file system.

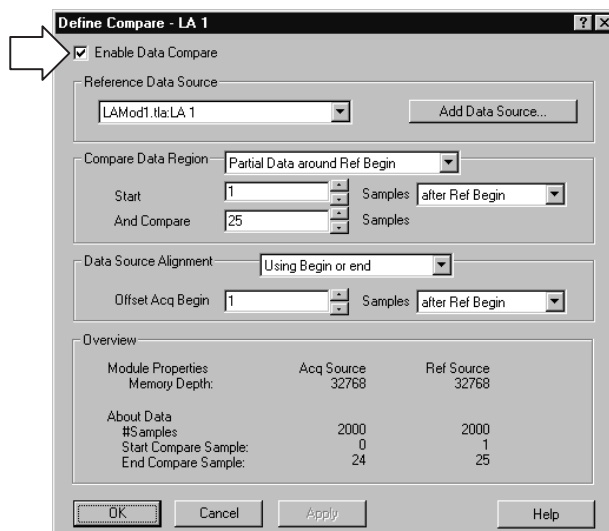


Figure 3–7: Enabling data compare

After you select the data source, define the amount of data that you want to compare against. You can compare all data or a portion of the data by filling in the appropriate information. You can also define the alignment of the data by filling in the appropriate information. A summary of your setup displays at the bottom of the dialog.

NOTE. After defining the compare setup, remember to select *Show Compare* in the Listing Window or Waveform Window property page.

Guidelines for Memory Compare. There are a few guidelines that you should be aware of when using memory compare:

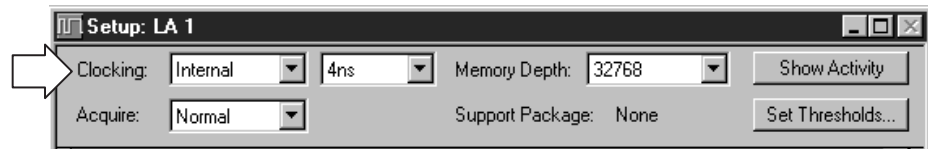
- You must enable the memory compare in the Compare Definition dialog box (see Figure 3–7).
- Acquisition modules and reference modules must be the same width.
- Specify the color of compare data in the Listing Window or Waveform Window property sheet, or use the default colors.
- You can search for data differences or data equalities.
- You can use memory compare with repetitive acquisitions.
- You can compare only the main LA data, you cannot compare glitch data, disassembler group data, or MagniVu data.

NOTE. Although you cannot compare disassembler group data directly, you can compare the raw nondisassembled data by using the channel groups as defined in the Setup window. To view these channel groups in a Listing window, use the Add Column tool bar button to add the channel group to the window.

Clocking

Use Clocking to specify the clock(s) used to sample data. Select one of two basic clocking modes, Internal (asynchronous) or External (synchronous). A third choice, Custom, is available if a microprocessor support package has been loaded. Your clocking choice determines further clocking selections.

Internal Clocking. Internal (asynchronous) clocking uses the LA module internal clock to determine when to sample data. Typically, internal clocking is used for timing analysis (waveform data).

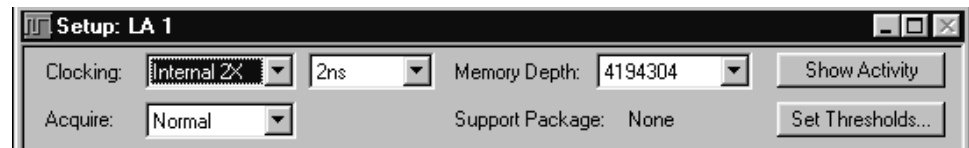


When you select Internal clocking, the only additional selection to make is the clock rate in the next field.

Because the internal clock signal is asynchronous to the target system, be careful to select a sample period that is considerably faster than the data rate of your target system.

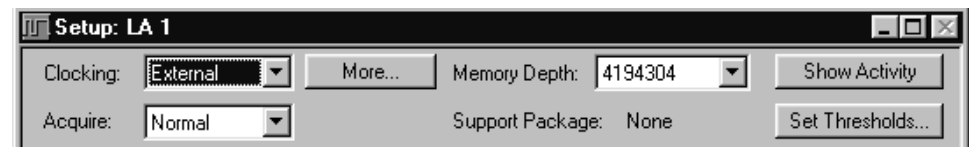
Internal 2x Clocking. Internal 2x Clocking provides 500 MHz timing on half channels with twice the memory depth. Use this mode for resolution less than 4 ns with full memory depth. However there is a trade-off for half the channels with twice memory depth at 2 ns. The 2 ns clock rate is a fixed clocking rate. You can use this mode with triggering and in both Listing and Waveform windows.

Refer to the online help for more information on Internal 2X clocking.



External Clocking. External (synchronous) clocking synchronizes data sampling with the clock of the target system so you can be more selective about the data you sample. This type of clocking is best for software analysis (listing data).

When you select External clocking, you have the option of further selections to define the sample clock. You can create clocking equations in the Clocking dialog box. Clocking equations qualify when data is sampled. The equations consist of a Boolean combination of events, linking clock and qualifier lines. Data is sampled and stored in memory only when this clock equation is true.



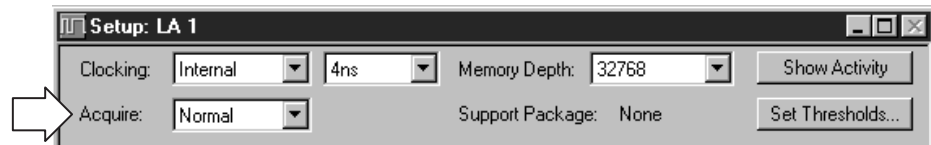
Advanced Clocking. Advanced clocking is available only if you select External clocking. Use advanced clocking to set up multiple-phase clocking, probe demultiplexing, and other clocking controls. Multiple-phase clocking specifies two different sample clock equations and assigns an equation to separate probe groups to clock in sample data. You can also sample data from different channel groups at different points in time relative to the sample clock through a variable setup and hold window.

For more information on advanced clocking, refer to the online help.

Custom Clocking. Custom clocking is used only with microprocessor support packages. Custom clocking enables and disables a variety of microprocessor-specific clock cycle types (such as DMA cycles). For more information, see the instructions that came with your microprocessor support package.

Selecting the Acquisition Mode

Use Acquire to select the acquisition mode. The acquisition mode determines the data to store. You can store channel data only, glitch data, or blocks of data around requested samples.



Normal Mode. Normal mode stores only the requested channel data.

Blocks Mode. Blocks mode stores a block of approximately 60 samples around each qualified sample. In Blocks mode, only channel data is stored. If you store blocks they will override other forms of data qualification. All samples in the block are always stored.

Glitch Mode (Internal Clocking Mode Only). Glitch mode captures glitch data and regular data for each data channel. You must select internal clocking for Glitch mode to be available.

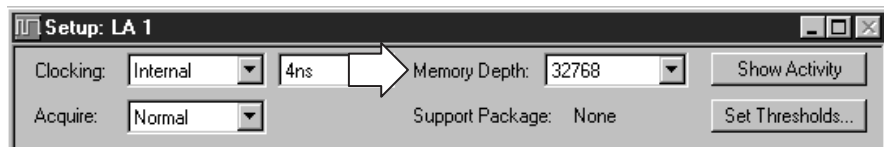
Glitch mode limits memory depth to half of the maximum depth and limits the sample period to 10 ns or greater. However there is no trade-off in channels which avoids changing probe connections.

Setting Memory Depth

Use Memory Depth to specify the total number of samples acquired by the LA module. If you do not require full memory depth, select a lesser value because you will have less data to search to find the data of interest.

For a given memory depth there is a tradeoff between the clock sample rate and data record length. (A faster sample rate provides a shorter time window, but with higher resolution.)

NOTE. If you select Glitch mode, the maximum memory depth is limited to one half the normal value.



Grouping Channels

Use channel grouping to organize the LA probe channels to match the configuration of the target system. Depending on your application, match the channel groups to the address and data buses, or other channels of interest. Then name the channel groups for easy identification.

Any number of groups can be created. Each group can contain any combination of module channels; the application does not restrict you from repeating channels from various groups.

When using group range events (range recognizers), the probe groups and probe channels must be used in hardware order. That is, probes must be used from the most-significant probe group to the least-significant probe group based on the following order:

C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3
CK2 CK1 CK0

The probe channels must be used from the most-significant channel to the least-significant probe channel based on the following order:

7 6 5 4 3 2 1 0

In 2x Clocking mode, half of the channels are colored out indicating they are unavailable (see Figure 3–8).

If a microprocessor support package is loaded, the channel groups are defined for you.

NOTE. If a microprocessor support package is loaded, you should not change or delete the default channel groups. Doing so can cause an inaccurate analysis. You can still add and delete new channel groups.

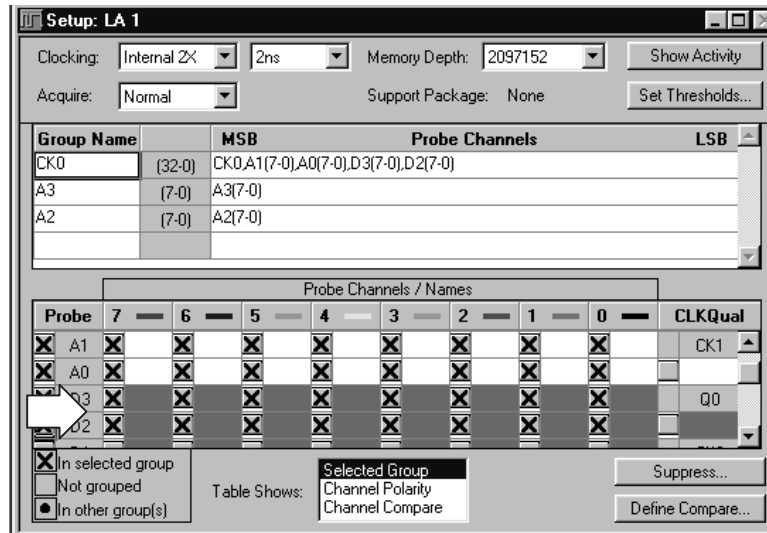


Figure 3–8: Colored-out channels in Internal 2x Clocking mode

Channel Group Name. Each channel group must have a name. Use the default name or enter another name. There is no limit to the number of groups. Channel groups defined in the channel grouping table are used in other displays and setup controls. The order of the groups in this table determine the order of presentation in other windows.

For each group name, list all the probe channels that make up the group. The group names are listed in the left column of the table. The individual probe channels that make up each group are listed in the right column of the table. The center column of the table lists the number of channels in a group (where a zero refers to bit 0). For example in Figure 3–9, the Address group is made up of 32 channels, with channel 31 as the most-significant bit (A3-7) and channel 0 as the least-significant bit (A0-0).

Probe Channels/Names Table. Use the Probe Channels/Names Table to enter names for individual channels, add and remove channels from a group, or change polarity of individual channels.

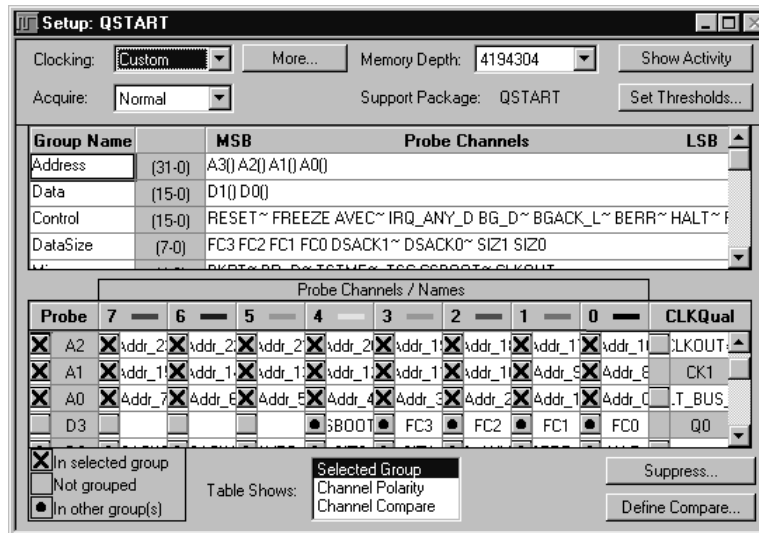


Figure 3-9: Channel grouping table in the Setup window

Activity Indicators

Use the Activity Indicators dialog box (click Show Activity in the LA Setup window) to show the real-time signal activity at the LA module probe tip without having to acquire data. The activity symbols indicate whether the signals at the probe tip are high, low, or changing. See Figure 3-10.

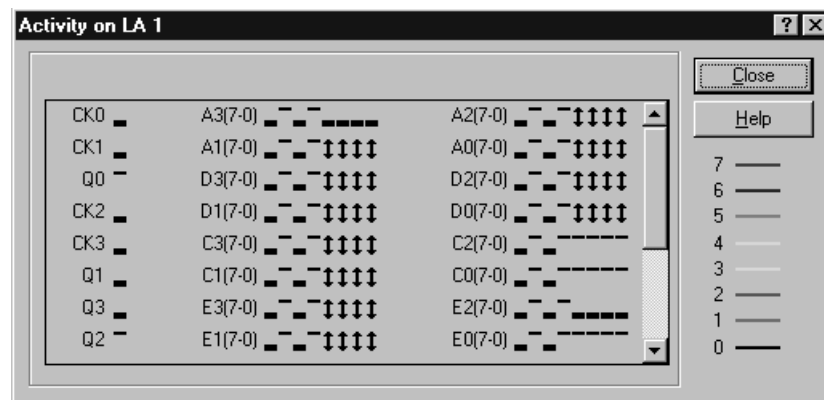


Figure 3-10: The Activity Indicators dialog box

If the activity indicators show no activity, the problem could be that there is no signal voltage, an incorrect threshold voltage level, or the channel lead is not connected. If all the channels associated with a probe are inactive, check the probe connections to the LA module.

You can leave the Activity Indicators dialog box open while you set up other windows. This dialog box is useful for verifying that clocks are active in external clocking and for troubleshooting complex clock setups.

Setting Probe Thresholds

Use Set Thresholds to set the input threshold voltage settings for probe channels, clocks, and qualifiers of the LA module. Changes are immediately executed even during acquisition. Figure 3–11 shows the Set Thresholds dialog box.

Initially, the Probe Thresholds box contains values that are set in the Preset page of the Options Property sheet.

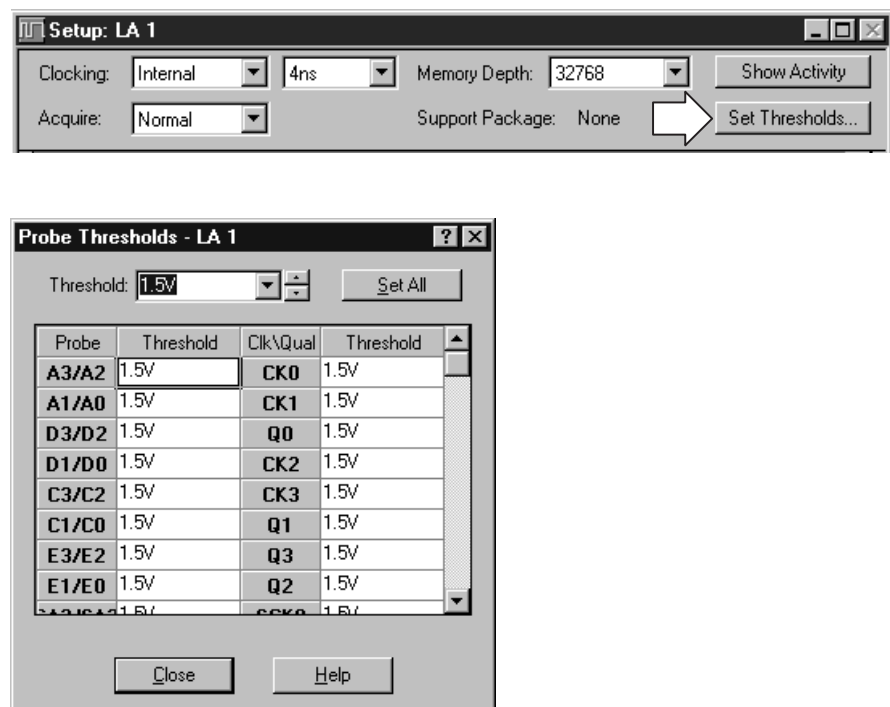


Figure 3–11: Probe Thresholds dialog box

Setting Up the Trigger Program

Use the LA Trigger window (see Figure 3–12) to construct a trigger program. You also use the Trigger window to select how and when to store data.

A trigger program is a series of events and actions that define when to trigger and store data. The trigger program filters acquired data to find a specific data event, or series of data events. The trigger program can accept information from other modules or send signals external to the logic analyzer.

Trigger programs range from simple to extremely complex. They are the key to logic analyzer operation, which is to acquire the desired data in acquisition memory and to display the data for viewing.

Once you become familiar with trigger programming, you can also create trigger programs without the help of the trigger library. For more information, see *Trigger Library* on page 3–17.

Before you work in the Trigger window, you should already have configured the LA module Setup window because some of the Setup window settings affect Trigger window selections.

Figure 3–12 shows a Trigger window with a trigger program loaded from the trigger library.

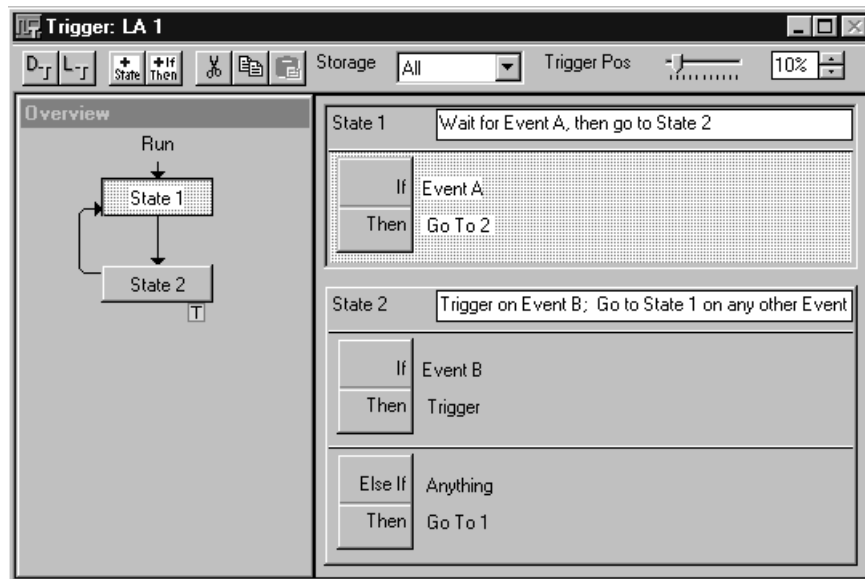


Figure 3–12: LA module Trigger window

Trigger Program Structure

A trigger program is made up of one or more states (up to 16). Only one state is active at a time.

Each state is made up of one or more clauses. If you use more than four trigger event resources in a state, you can have up to four clauses per state. If you have four or fewer trigger event resources in a state, you can define up to 16 clauses per state.

Clauses are made up of two parts: an If statement, that defines the data event of interest, and the Then statement, which specifies the action taken when the If statement is true. You can define up to eight events per If statement and up to eight trigger actions per Then statement.

During each sample clock cycle, all clauses within the active state simultaneously evaluate each data sample. Clauses are evaluated from top (State #1, IF-Then Clause #1) to bottom. When one of the clauses goes true (the event defined in the If statement occurs), then the logic analyzer performs the action(s) specified in the Then statement. There are several actions to choose from, including triggering the system and transferring control of the trigger program to another state.

NOTE. *If multiple clauses are true in the same clock cycle, only the earliest clause in the sequence to go true will have its action(s) executed.*

Trigger Window Structure

The Trigger window summarizes the trigger program. The Overview shows the general structure of the trigger program. The Trigger Detail, at the right of the window, summarizes activity within individual program states. You can click the If/Then button in the Trigger Detail to open the Clause Definition dialog box, which is where the actual trigger programming takes place.

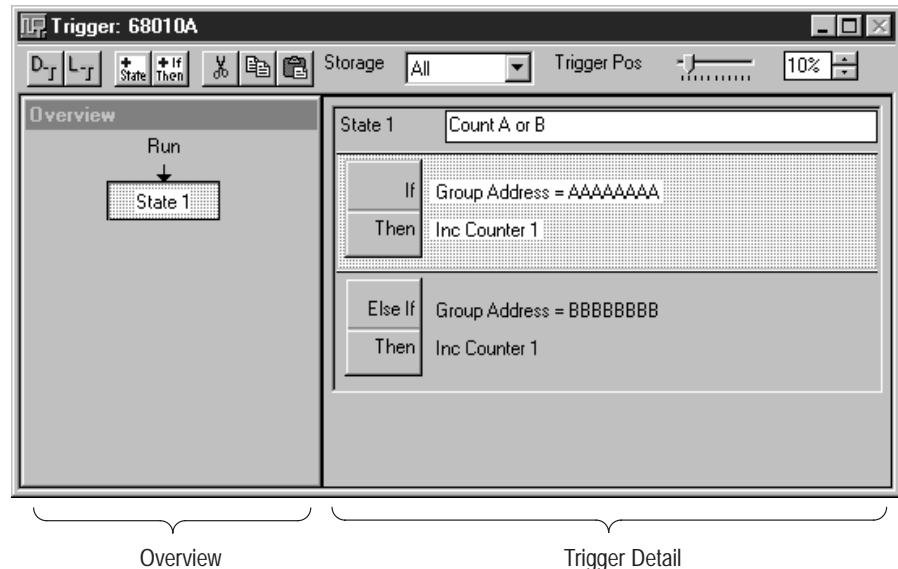


Figure 3–13: Trigger window structure

Overview. The Overview portion of the Trigger window shows the relationship of the states. See Figure 3–14. This example shows a branch occurring in State 2. This example also shows that a trigger (note the trigger indicator) occurs in State 2 and an Arm occurs.

To view the details in a particular state, double-click on the State button in the Overview.

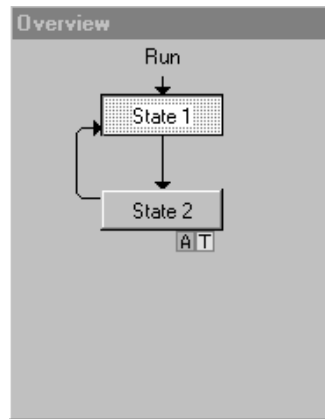


Figure 3–14: Overview portion of LA Trigger window

You can view the progress of the trigger states during acquisition using the Status Monitor. (See *Viewing Acquisition Activity* on page 3–53.)

Trigger Detail. The Trigger Detail portion, at the right of the Trigger window, shows summary information about the clauses within the states. See Figure 3–15. For lengthy trigger programs, click on the State buttons in the Overview to jump to the corresponding Trigger Details.

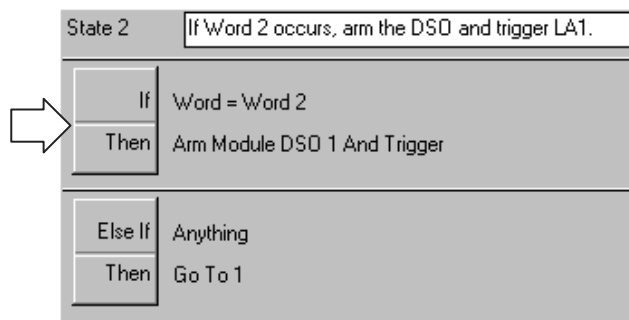


Figure 3–15: Trigger detail portion of LA Trigger window

Click on the If/Then button to open the Clause Definition dialog box for complete information about the clause.

Trigger Library

One advantage of a logic analyzer is that you can create sophisticated trigger programs so that you can carefully qualify and store only the relevant data.

This process is simplified with the trigger library. The trigger library provides a list of trigger programs to fit most needs. The trigger programming is partially done for you. Select a trigger program that is close to what you require, and then alter the program as necessary. Once you have customized the trigger, you can save it along with the rest of your setup using the Save Module or Save System function. You can later retrieve the saved trigger program alone or with the related saved module or system information. For instructions on accessing the trigger library refer to *Loading a Trigger from the Trigger Library* beginning on page 3–19.

Table 3–1 lists the programs in the trigger library and a brief description of each library item.

Table 3–1: LA Trigger library

File name	Description
TrigOnA	Trigger on the first occurrence of Event A.
TrigOnAafterN	Wait for Event A. Trigger after the specified number of events.
TrigOnNthA	Trigger after Event A has occurred a specified number of times.
TrigOnNthAorB	Trigger after Event A or Event B has occurred a specified number of times.
TrigOnAthenB	Trigger if Event B eventually follows Event A.
TrigOnAimedB	Trigger if Event B immediately follows Event A.
TrigOnAthenBresetC	Wait for Event A. If Event C occurs before Event B, then reset and wait for Event A again. Otherwise, trigger when Event B occurs.
TrigOnAtoBltnCs	Trigger on Event C if Event C occurs less than or equal to the specified number of times between Event A and Event B.
TrigOnAtoBgtNCs	Trigger on Event C if Event C occurs more than the specified number of times between Event A and Event B.
TrigOnAthenBinN	Trigger when Event B occurs within a specified number of events of Event A.
TrigOnAinRange	Trigger when the group event occurs within specified upper and lower ranges.
TrigOnGlitch	Trigger on glitches; valid only with Internal clocking.
TrigOnSetHold	Trigger on setup and hold violations; valid only with External or Custom clocking.

Table 3–1: LA Trigger library (Cont.)

File name	Description
TrigOnAtoBinT	Trigger when Event B follows Event A within the specified time.
TrigOnAtoBafterT	Trigger when Event B follows Event A after the specified time.
CountA	Count the occurrences of Event A. This program does not trigger the logic analyzer.
CountAorB	Count the occurrences of Event A or Event B. This program does not trigger the logic analyzer.
CountCfromAtoB	Count the occurrences of Event C between Event A and Event B. This program does not trigger the logic analyzer.
AccumCfromAtoB	Accumulate the total counts of Event C between Event A and Event B. This program does not trigger the logic analyzer.
AccumTfromAtoB	Accumulate the total time between Event A and Event B. This program does not trigger the logic analyzer.
AccumTinRange	Accumulate the total time spent within the specified range in Event A. This program does not trigger the logic analyzer.
AccumToutRange	Accumulate the total time spent outside the specified range in Event A. This program does not trigger the logic analyzer.
TimeBetweenAandB	Measure the delay between Event A and Event B. This program does not trigger the logic analyzer.
TimeInRange	Measure the time spent within a specific range of events. This program does not trigger the logic analyzer.
TimeOutRange	Measure the time spent outside a specific range of events. This program does not trigger the logic analyzer.
StoreOnA	Store nothing except occurrences of Event A. This program does not trigger the logic analyzer.
StoreOnAorB	Store nothing except occurrences of Event A or Event B. This program does not trigger the logic analyzer.
StoreFromAtoB	Store nothing except the samples between Event A and Event B. This program does not trigger the logic analyzer.
StoreExceptAtoB	Store everything except those samples between Event A and Event B. This program does not trigger the logic analyzer.
StoreInRange	Store nothing except samples within specified ranges of Event A. This program does not trigger the logic analyzer.
TrigOnSignal	Trigger on a signal from another module.
SendSignal	Send a signal to another module when Event A occurs.
TrigSysOnA	Trigger the system when Event A occurs.

Loading a Trigger from the Trigger Library

To load a trigger program from the trigger library, follow these steps:

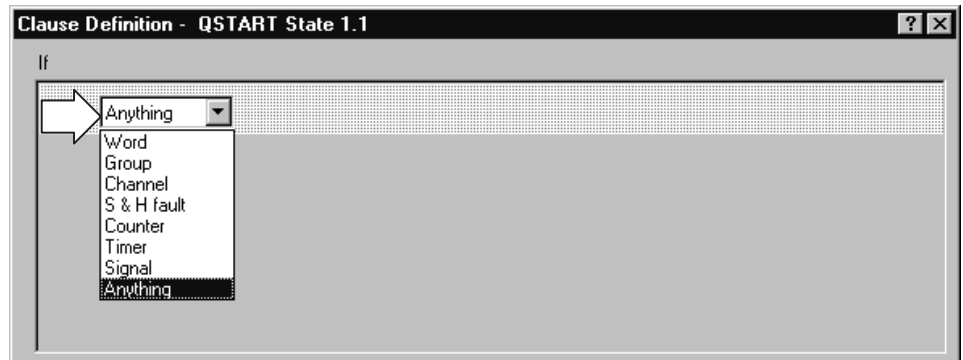
1. From the Trigger window, click the Load Trigger toolbar button.



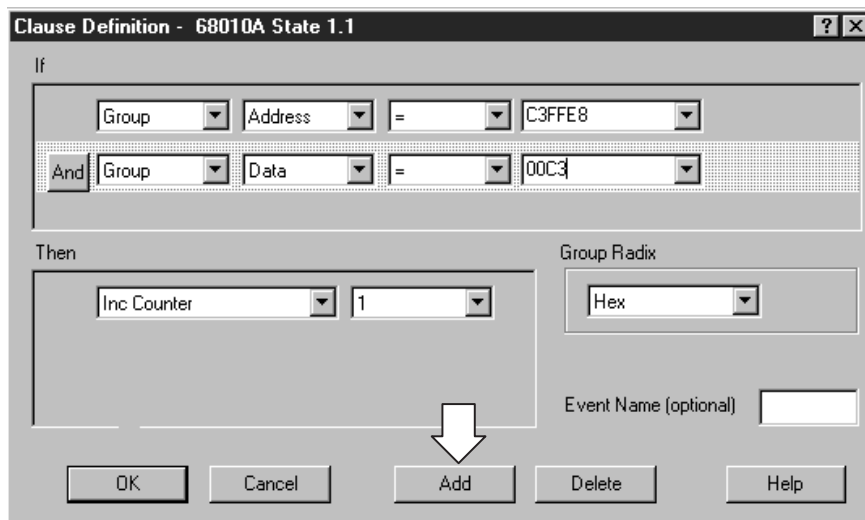
2. From the Load LA Trigger dialog box, click Browse Library.
3. Select a trigger program from the list.
4. Click Open to apply the selection.
5. Click Load to load the trigger program into the module.

Once you load the trigger program, customize it for your application.

6. Click the If/Then button to open the Clause Definition dialog box. This is where you specify trigger program details.
7. Change the Clause Definition selections to fit your application. Start with the first box in the If statement; the selection you make affects other selections. Enter appropriate values in the address and data boxes.



8. If you want additional clauses, you can add to the If or Then statements using the Add button, as shown in the following figure.



9. Click OK to complete the clause definition.
10. Check the trigger program summary in the Trigger window.

Trigger Events Use trigger events to define the If portion of the event clause in the trigger program. Table 3–2 lists the trigger events available.

Table 3–2: Trigger events

Event	Description
Word	Tests the channel groups for the word values defined in the Word definition dialog box.
Group	Tests a specified channel group for a specific value, a range of values, or a value change.
Channel	Tests the specified channel for a value or a value change.
Glitch	Detects glitches in channel groups as defined in the Glitch Detect dialog box. Only available with internal (asynchronous) clocking.
Setup & Hold fault	Tests setup and hold parameters as defined in the Setup and Hold Event dialog box. Not available as an event with internal (asynchronous) clocking.
Counter and timer events	Tests the specified counter or timer value. Timer events are supported by all LA Modules except TLA7Lx and TLA7Mx modules with serial numbers B019999 or lower.
Signal	Looks for one of the four internal system signals. Only one signal event is available in a trigger program.
Anything	All sampled data makes this event true.
Nothing	All sampled data makes this event false.

Trigger Resources You can use up to 16 unique trigger resources (not including counters and timers) in a trigger program to define the events and actions. A trigger resource can be used more than once in a trigger program. However, some events use more than one trigger resource. Table 3–3 lists the trigger resources and any interactions that may occur when you use them.

Table 3–3: Trigger resources

Resource	Operator	Interactions and restrictions
Word	=, Is Not	One trigger resource across all defined channel groups.
Group		
Word recognizer	=, Is Not	One trigger resource per channel group.
Range recognizer	<, <=, >=, >, Is In, Is Not In	Three trigger resources per channel group.
Change detector	Changes	One trigger resource per group event, one change detector allowed in a trigger program, not available when transitional storage is used.
Channel		
Word recognizer	=	One trigger resource per channel group.
Change detector	Goes, Doesn't go	One trigger resource, one change detector allowed in a trigger program, not available when transitional storage is used.
Glitch		One trigger resource, only available with internal (asynchronous) clocking.
Setup & Hold Fault		One trigger resource, only available with external (synchronous) or custom clocking.
Counter	>, <=	0 trigger resources, 2 counters or 2 timers. Maximum width 51 bits Maximum clocking 250 MHz Maximum count $2^{51} - 1$ Counter 1 and 2 events conflict with Timer 1 and 2 events respectively.
Timer	>, <=	0 trigger resources, 2 counters or 2 timers Maximum width 51 bits Maximum clocking 250 MHz Maximum time 2,000,000 S (23 days) Counter 1 and 2 events conflict with Timer 1 and 2 events respectively.
Signal (Signal in)	Is True, Is False	One trigger resource, uses one of four system signals. Only one signal event is available in a trigger program.
Anything		0 trigger resources. Used as a placeholder. Not available with the OR conjunction.
Nothing		0 trigger resources. Used as a placeholder with the OR conjunction.

Trigger Actions After defining the events in the If (event) portion of the clause, you can select one or more trigger actions to complete the clause. Table 3–4 lists the trigger actions available for your trigger program.

Table 3–4: Trigger actions

Action	Description
Trigger	Triggers the current module. When you use Trigger in the trigger program, you cannot use Trigger All Modules.
Trigger All Modules	Also known as a System trigger. This signal is also available at the System Trigger Out connector. When you use Trigger All Modules in the trigger program, you cannot use Trigger.
Go To	Passes the program flow to a different trigger state. You can only use one Go To action in the clause definition.
Counter and Timer actions	Starts, stops, resets, or clears counters or timers. Counter 1 and 2 actions conflict with Timer 1 and 2 actions respectively. Counter/timer actions may conflict with counter/timer event usage.
Set and Clear Signal	Sets or clears one of the four internal system signals. You can use only one Set or Clear in a trigger program. The Set or Clear Signal is mutually exclusive with the Arm Module action.
Arm Module	Sends an Arm signal to another module. The other module begins running its trigger program. You can arm only one module in a trigger program. However, you can use actions throughout the trigger program. Arm Module is mutually exclusive with Set and Clear Signal actions.
Store Sample	Stores exactly one sample. Not available in Start/Stop storage mode.
Start & Stop Storing	Begins or ends storing of samples. Start and Stop Storing actions only appear when you select Start/Stop storage mode. Use Start and Stop Storing in conjunction with Start/Stop storage mode in the Trigger window. Available only in Start/Stop storage mode.
Do Nothing	Use as a placeholder when defining a complicated trigger program. Does not override other actions specified in a clause.

Other Trigger Options

From the Trigger window, you can also make data storage and trigger position selections.

Storage. Use the storage selections to avoid filling up the acquisition memory with data samples that do not interest you. You can use the storage selections to disqualify the unwanted data samples and fill memory only with the desired data.

Use the Storage box to select the default data storage rules for the module. Use one of the storage actions in the Then statement of the clause definition to override the default storage setting.

The example shown in Figure 3–16 is using conditional storage. Data is stored only when the specified event is true.

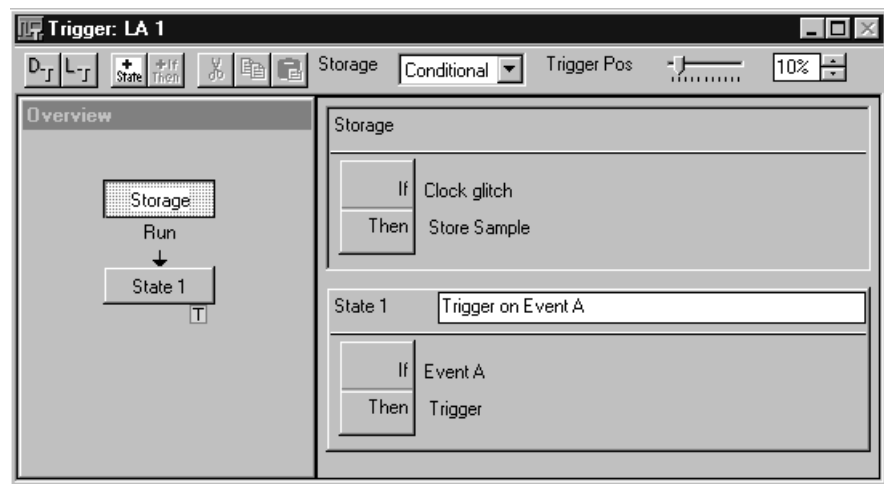


Figure 3–16: Using trigger storage

Trigger Position. The Trigger Position selects the amount of posttrigger data that is stored and determines the position of the trigger in the data record.

After a module has triggered, it continues to acquire data until it fills a specified amount of memory. The total memory depth that the module fills is set in the Memory Depth box in the Setup window. The proportion of data that is stored before and after the trigger is determined by the Trigger Position field. For example, if the Trigger Position is set to 10%, and the module triggers, then the module continues to acquire post trigger data until the remaining 90% of memory is filled.

If the trigger event occurs on any data sample before the specified amount of pretrigger data has occurred, then the logic analyzer triggers and begins filling memory with post trigger data regardless of the amount of pretrigger data specified. For example, if you set the trigger position to 50% and set the logic analyzer to trigger on a processor reset, start the logic analyzer, then power on your target system, the logic analyzer will trigger. However, the logic analyzer memory will be filled only with post trigger data, not any pretrigger data. This is due to the trigger event, which has higher precedence, occurring before the pretrigger condition is satisfied.

Saving Trigger Programs

You can save your trigger programs for future use by means of the Save Module or Save System functions. Although these functions save more than just the trigger program, you can load just the trigger program from one of the saved files. For more information, see *Saving and Loading Setups, Triggers, and Data* on page 3–44.

Setting Up the DSO Module

Before acquiring and displaying an analog waveform, you must first set up the DSO using the DSO Setup window. You can set the vertical, horizontal, and trigger parameters manually, or you can use Autoset for a quick automatic setup based on the input signal.

NOTE. *The setup and data windows operate independently; you cannot change setup parameters by changing the data display. Once you acquire data, you can manipulate the display, but that will not change the input settings used to acquire the data. You must return to the DSO Setup window to change input settings which take effect with the next acquisition.*

To open the DSO Setup window, go to the System window and click the DSO Setup button.

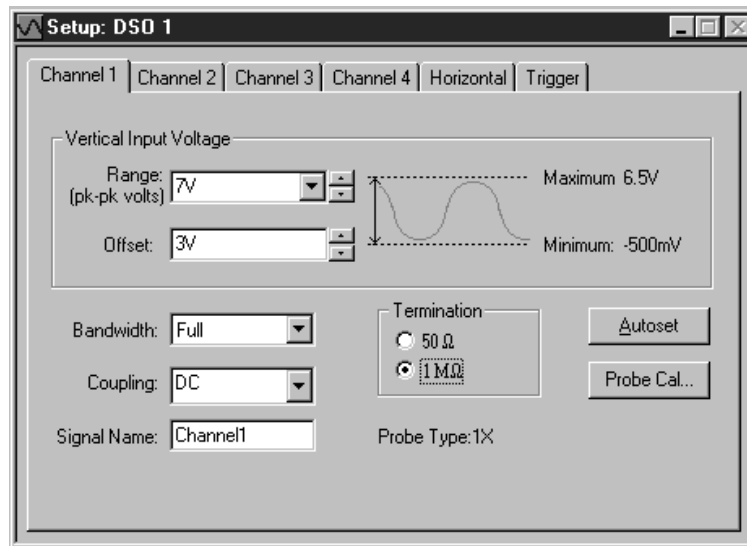


Figure 3-17: DSO Setup window

DSO Probe Calibration

Probe calibration optimizes the signal path for this probe/channel/module combination. For maximum accuracy, execute Probe Cal if any of these conditions have occurred:

- The ambient temperature has changed more than 5°C
- You reconnect the probes to different DSO module input channels

The Probe Calibration dialog controls all DSO probe calibration cycles and directs you to perform any necessary steps. You can calibrate all attached probes or only the probe on the selected channel.

NOTE. *Passive or unknown probes are not calibrated.*

You can start a calibration cycle, view the progress of calibration, and see the results of calibration. Once calibration starts, the calibration cycle of a single probe cannot be stopped. After a calibration cycle completes, you can see the status of probe calibration.

To open the Probe Calibration dialog, go to the System window and click the DSO Setup button, select a vertical tab (Channel x), and click Probe Cal.

NOTE. You should execute the DSO module self calibration if the ambient operating temperature has changed more than 5° C since last calibration. Also, you should execute the self calibration once a week if vertical settings of 50 mV full scale or less are used. Perform self calibration after a 30 minute warm up.

To open the Self Calibration property page, go to the System menu and select Calibration and Diagnostics. Click Self Calibration.

Autoset

Use Autoset when you need to see a signal in a circuit, but do not know the signal amplitude or frequency. Autoset automatically chooses the DSO setup values based on the input signal at the time you clicked the Autoset button.

Autoset works best on repetitive signals that do not have a DC offset component. If the Autoset setup does not display the waveform as you want it, you can easily change the setup manually.

To set the DSO input values based on the input signal:

1. Go to the System window and click the DSO Setup button.
2. Click Autoset from any page of the DSO Setup window.

The Autoset selections apply to all input channels, the horizontal setup, and the trigger setup, regardless of which Autoset button was clicked.

3. If the signal changes, or you move the probe to another signal, click Autoset again to reset the setup values.

Autoset affects only the DSO setup; it does not affect data window settings. You may need to adjust data window settings for optimum display of the data.

Vertical Controls

Use the vertical controls to adjust vertical input voltage parameters. See Figure 3–18.

To open the page containing the vertical controls, go to the System window and click the DSO Setup button and then select one of the Channel tabs.

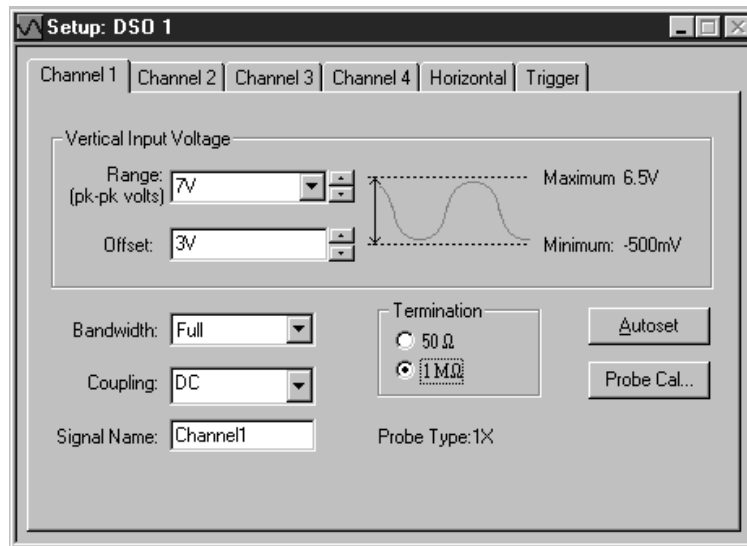


Figure 3–18: DSO Setup window vertical input settings

For best vertical resolution, set the range just slightly larger than the expected input signal. Autoset automatically sets the vertical range for the signal, assuming a 0 VDC offset.

Offset. Offset is the offset voltage applied to the probe. If Range is changed using the preset values, then Range also sets the Offset. The Offset default is 3 V for TTL signals.

Bandwidth. Bandwidth is the range of frequencies that can be acquired and displayed accurately. Your bandwidth selection sets the upper limit of frequencies that will be acquired and displayed. Bandwidth filters reduce unwanted noise and aliasing.

Coupling. Coupling selects how the input signal is coupled to the vertical input channel.

Horizontal Controls

Horizontal settings control the rate at which the data is sampled and the amount of data acquired. See Figure 3–19.

To open the horizontal page, go to the System window, click the DSO Setup button, and then select the Horizontal tab.

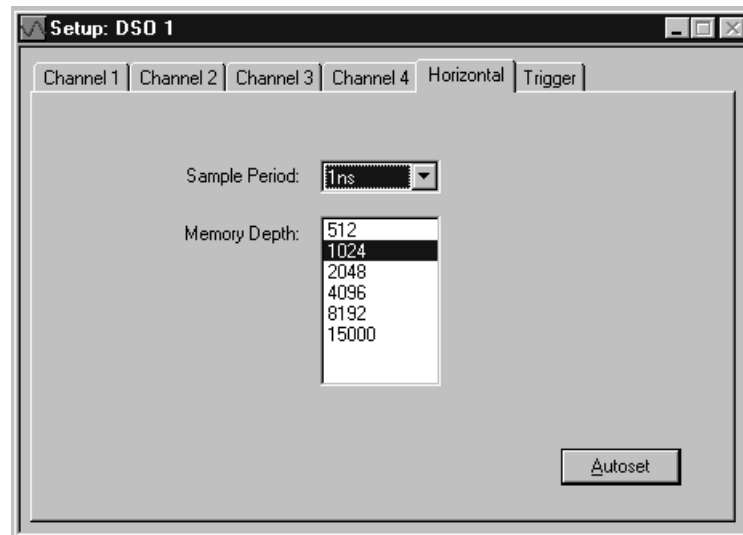


Figure 3–19: DSO Setup window Horizontal settings

Sample Period. The Sample Period sets the interval between successive samples in a waveform record. Choose a sample period that is fast enough that the waveform will not be aliased, and slow enough to provide the waveform record length that you need. For repetitive waveforms, you should set the sample period to at least five times faster than that of the waveform.

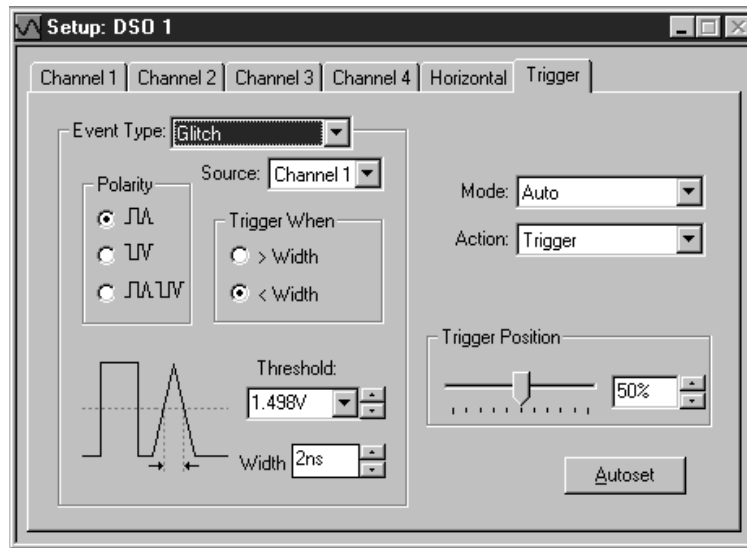
Memory Depth. The Memory Depth sets the total number of data samples to be acquired. If you do not need to use the full memory depth to acquire the data of interest, select a smaller memory depth to get faster acquisitions.

Trigger

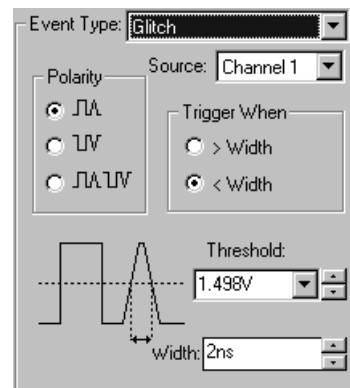
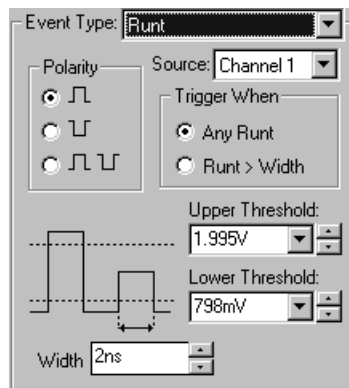
The DSO Trigger page contains all controls for setting DSO trigger events and actions. Threshold changes are recognized and executed immediately during acquisitions. Execution of all other controls are delayed until the next acquisition.

To open the Trigger setup page, go to the System window and click the DSO Trigger button.

Select a trigger event from the list of event types, and then modify it for your application.



Event Type. Event Type selects the type of event the DSO will recognize as a trigger. Choose from the list of trigger event types. The following figure shows two of the available trigger event selections.

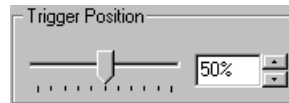


Mode. Mode selects whether the DSO waits for a trigger (Normal) or forces a trigger after a set length of time has passed without a trigger (Auto).

Action. Action selects what happens when a trigger is recognized. Choose from a list of actions. Actions include triggering the DSO, triggering all modules, or triggering and arming another module.

Trigger Position. Trigger position sets the amount of data in the data record that occurs before the trigger.

To set the Trigger Position, use the slider or enter a numeric value, as shown below.



Event-Based Selections. Depending on the trigger event you choose, other selections may become available. Refer to the online help for further information.

Setting Up the Pattern Generator Module

The pattern generator modules, like the LA modules, have a Setup window where you can specify the individual module setups, channel setups, probe setups, and signal setups. You should define these parameters before setting up the pattern generator program in the Program window.

Module Setup Window

Use the Module Setup window to define the channel mode, Run mode, clocking, and event setups.

- Use the channel mode to select the speed and width of the logical module. Define the channel mode before defining other parameters, otherwise all module information will be lost when you change the channel mode.
- Set the Run mode to Step to output the patterns vectors one at a time. Use the Step button in the Status Monitor window to advance the steps. Set the Run mode to Continuous to output all vectors in a single step.
- Select the Hi-Z on Stop to cause the probes data and strobe outputs to go to a high-impedance state when the program stops.
- Use the Clocking to select an internal or external clock. When you select an external clock, you can also select the polarity and the threshold levels.
- Use the Event setups to filter out events, enable inhibit functions, and to define whether the pattern generator responds to events due to edges or levels.

Figure 3–20 shows an example of the Module Setup window.

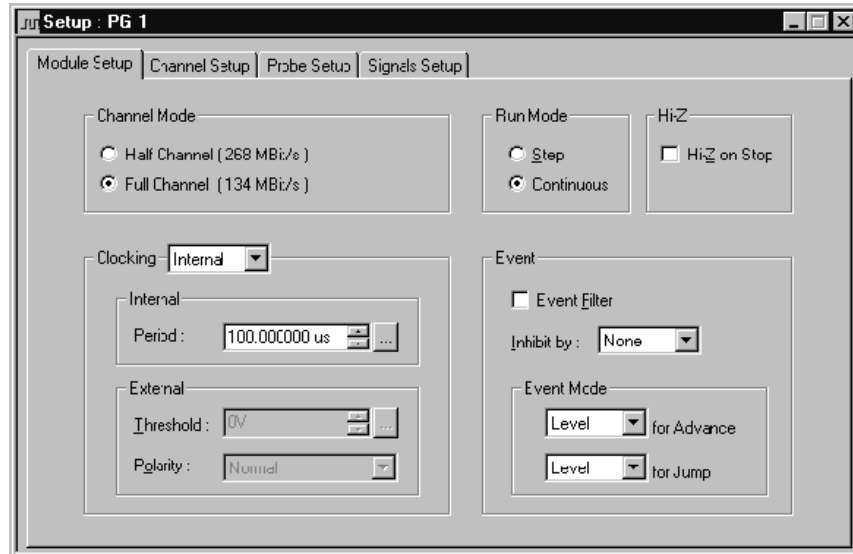


Figure 3–20: Module Setup window

Channel Setup Window

The Channel Setup window functions similar to the Channel Setup window in the LA modules. Use this window to define the channel group names, the logical grouping of channels, and the individual channel names. Figure 3–21 shows an example of the Channel Setup window.

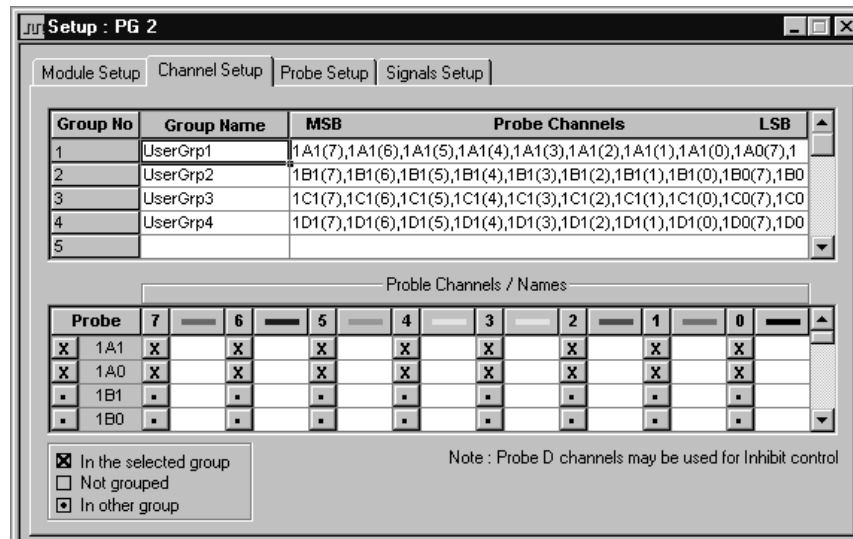
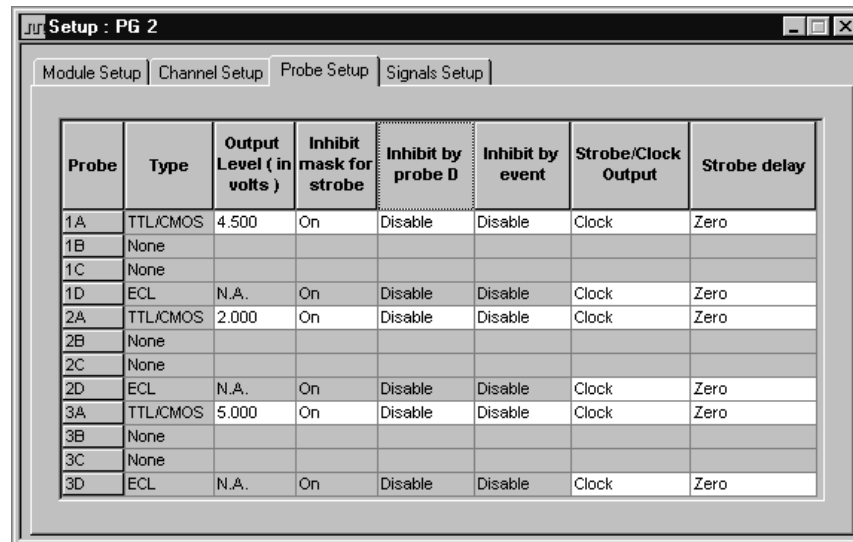


Figure 3–21: Channel Setup window

Probe Setup Window

Use the Probe Setup window to specify the probe details such as the output threshold voltage and inhibit information. Figure 3–22 shows an example of the Probe Setup window.



The screenshot shows a software window titled "Setup : PG 2" with tabs for "Module Setup", "Channel Setup", "Probe Setup", and "Signals Setup". The "Probe Setup" tab is active, displaying a table with the following data:

Probe	Type	Output Level (in volts)	Inhibit mask for strobe	Inhibit by probe D	Inhibit by event	Strobe/Clock Output	Strobe delay
1A	TTL/CMOS	4.500	On	Disable	Disable	Clock	Zero
1B	None						
1C	None						
1D	ECL	N.A.	On	Disable	Disable	Clock	Zero
2A	TTL/CMOS	2.000	On	Disable	Disable	Clock	Zero
2B	None						
2C	None						
2D	ECL	N.A.	On	Disable	Disable	Clock	Zero
3A	TTL/CMOS	5.000	On	Disable	Disable	Clock	Zero
3B	None						
3C	None						
3D	ECL	N.A.	On	Disable	Disable	Clock	Zero

Figure 3–22: Probe Setup window

Signal Setup Window

Use the Signal Setup window to define the input and output signals. After defining these signals, you can use them in the Program window to control the flow of the pattern generator program. You can use one of the backplane signals as an input to the pattern generator module and another backplane signal as an output signal. For more information on using signals, refer to *Intermodule and External Signaling* beginning on page 3–41.

Figure 3–23 shows an example of the Signal Setup window.

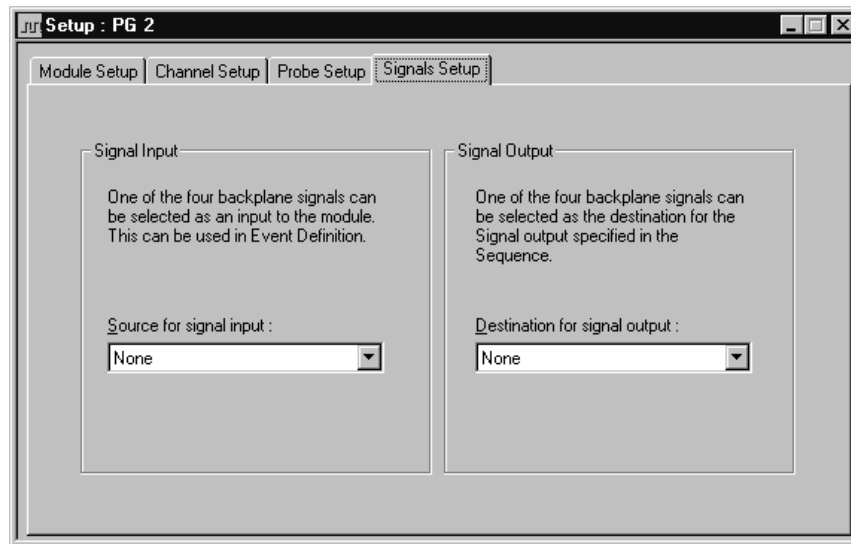


Figure 3–23: Signals Setup window

Setting Up the Pattern Generator Program

After you have defined the module setups, you can then use the Program window to define the pattern generator program. Use the Program windows in the following sequence:

1. Use the Block Definition window together with the Listing or Waveform window to define the data blocks and the vectors in each block.
2. Use the Sequence Definition window to define a high-level sequence flow of the pattern generator program.
3. Use the Subsequence Definition window to define subsequences or macros. You can call these subsequences in the Sequence Definition window.
4. Use the Event Definition window to define how events are used with the pattern generator program.

Block Definition Window

Use the Block definition window to define blocks of output data. You can define the size of each block and assign each block a meaningful name (such as Init, Read Cycle, Interrupt). Each block has its own associated Listing or Waveform window. Figure 3–24 shows an example of the Block Definition window.

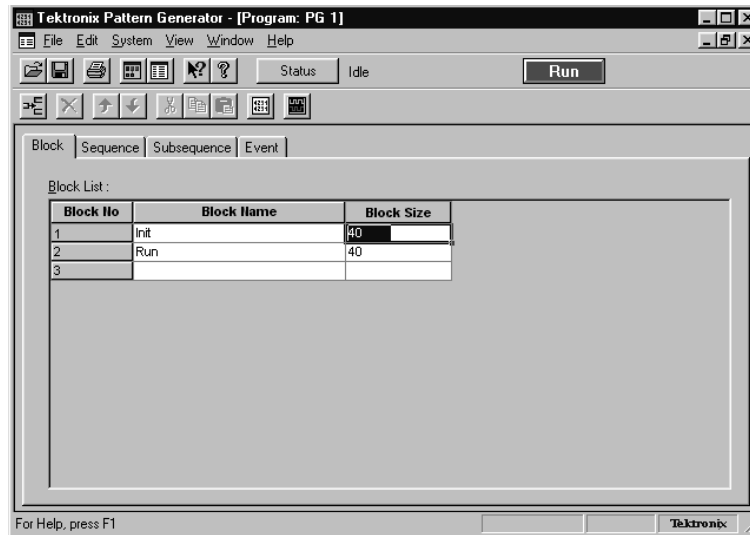


Figure 3–24: Block Definition window

Use the Listing and Waveform windows to enter the data vectors. Click on the Listing window icon to open the Listing window for the current block and enter the vector data. You can edit the vectors in either the Listing or Waveform windows.

Sequence Definition Window

After defining the data blocks, use the Sequence Definition window to create a high-level overview of the pattern generator program. You can do the following tasks with sequences.

- Output the data blocks. Use the data blocks that you defined in the Block Definition window. You can specify how many times you want to output the data blocks.
- Determine the program flow. You can wait for an external event to occur before outputting the data blocks. You can also pass the program control to another sequence by jumping to a specific sequence label.
- Use Subsequences to execute or control the program flow. Subsequences are macros that you define in the Subsequence Definition window. For example, you can use a subsequence to output a read cycle five times and then output a write cycle before returning control to the main program sequence.
- Output a high or low signal to a defined event line. The event line is the one you defined in the Signal Setup window.

Each sequence has its own line. Use labels for each line to help with the program flow. Unless you set up a data block to be repeated an infinite number of times, the program flow will pass to the next sequence (or jump to a defined label). When the last sequence has been executed the program flow stops. Figure 3–25 shows an example of the Sequence Definition window.

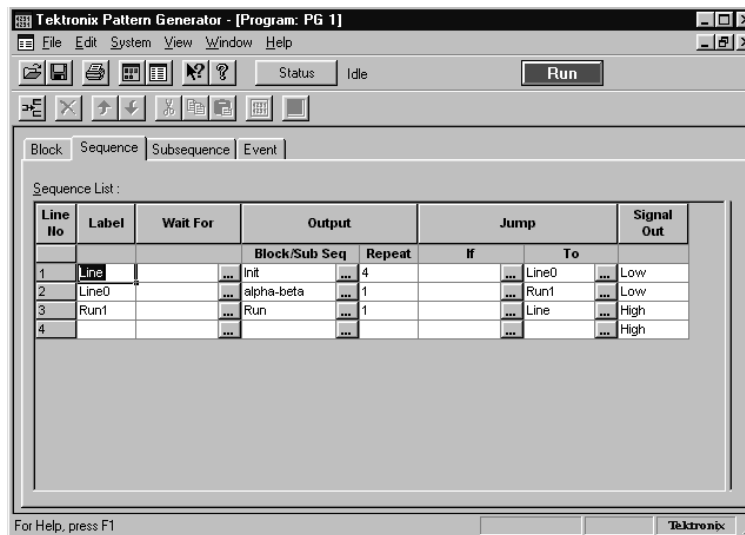


Figure 3–25: Sequence Definition window

After defining a sequence you can display a graphical image of the sequence flow by clicking and dragging the vertical bar on right side of the Sequence Definition window (see Figure 3–26).

The appearance of the sequence flow depends on the sequence definition. Each sequence line has its graphic (see Figure 3–27).

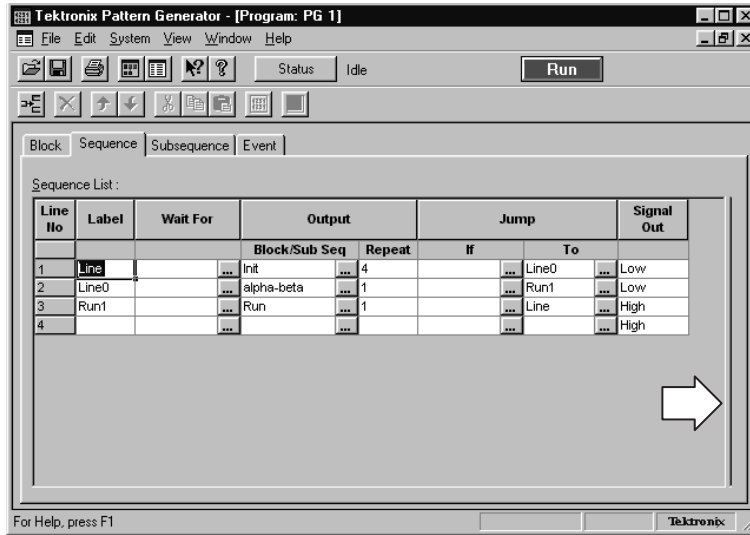


Figure 3–26: Drag the vertical bar to the left to display the sequence flow graphic

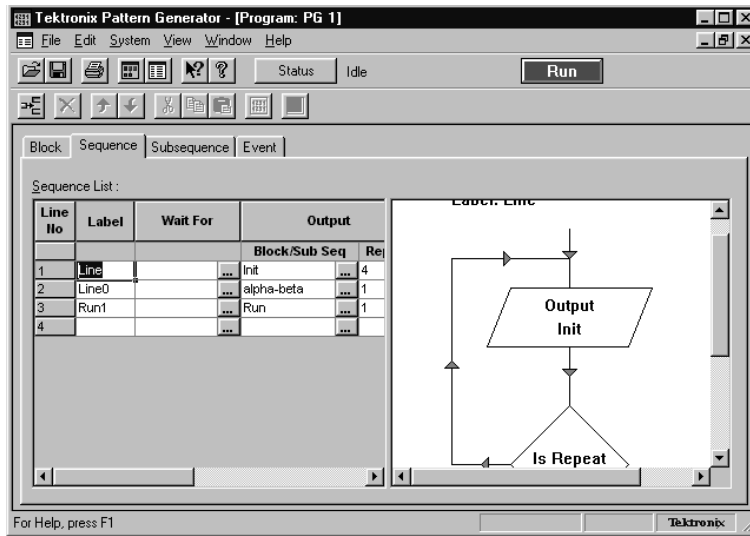


Figure 3–27: Sequence flow graphic

Subsequence Definition Window

Use the Subsequence Definition window to define macros to use in the Sequence Definition window. Subsequences are useful for defining tasks that you may not want to appear directly in the Sequence Definition window.

Assign a name for the subsequence in the left side of the window. This name will appear in the Sequence Definition window. Define the actual tasks (data blocks) in the right side of the window. The block names are the ones you defined in the Block Definition window. Figure 3–28 shows an example of the Subsequence Definition window.

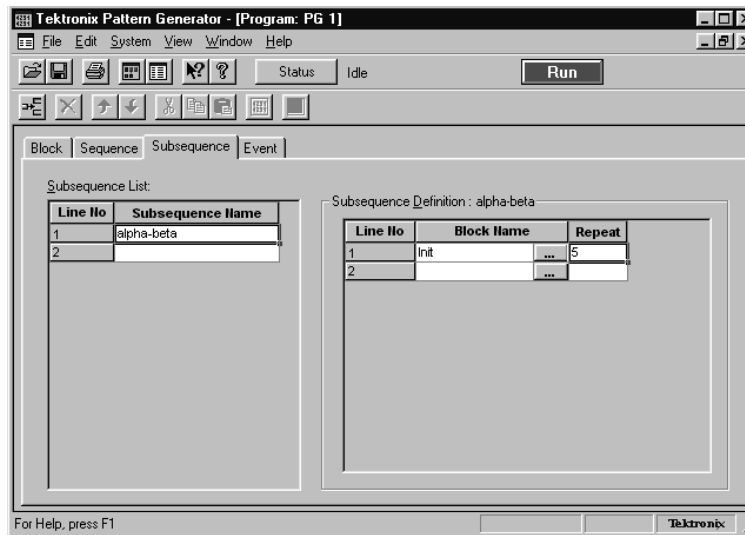


Figure 3–28: Subsequence Definition window

Event Definition Window

Use the Event Definition window to define events that you can use in the Sequence Definition window. Enter an event name in the left side of the window and then define events in the right side of the window.

Signal events refer to the input backplane input signal that you defined in the Signal Setups window. The Probe events refer to the input signals on each probe; each probe can have two event lines. Figure 3–29 shows an example of the Event Definition window.

The events in each row are logically ANDed together while the rows are logically ORed together.

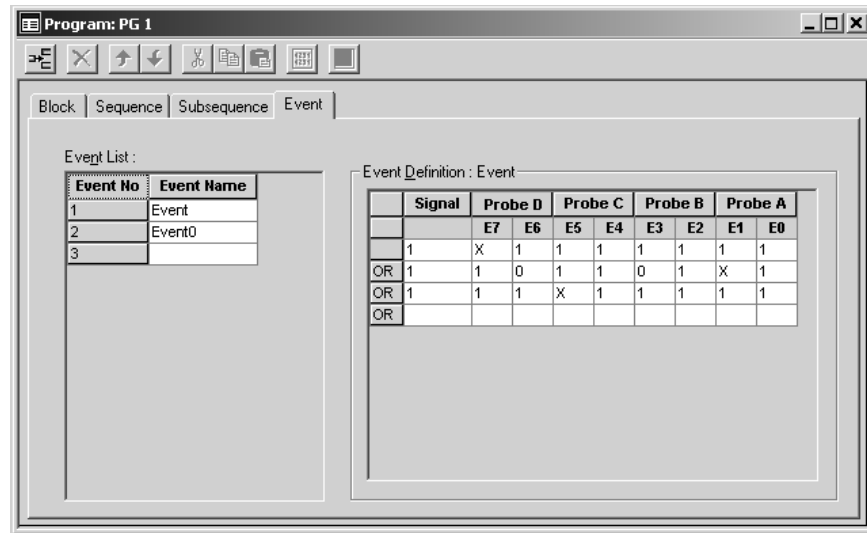


Figure 3–29: Event Definition window

System Trigger

The system trigger is a global trigger event that forces all untriggered modules to arm immediately and trigger. Only one system trigger occurs per acquisition. When displaying data, the logic analyzer uses the system trigger as the primary reference point for the acquisition. The data windows show the system trigger and all module triggers. Module triggers can be forced by the system trigger or specified by module trigger programs.

The system trigger can be generated from any of several sources. Often, the system trigger is specified in a module's trigger program. Any module can specify the system trigger as a trigger action (Trigger All Modules). However, modules can specify trigger actions other than system triggers, and the system trigger does not have to originate from a module. The logic analyzer can also accept a system trigger generated by an external source. External system triggers are input through the SYSTEM TRIG IN connector. Regardless of the source of the system trigger, all modules must respond.

It is not uncommon to have a condition where the acquisition completed, but where an explicit system trigger did not occur. (This means that there was neither an external system trigger, nor a system trigger generated internally by a module trigger program.) To ensure that a time reference exists for the acquisition, the logic analyzer must designate a system trigger. If no system trigger is generated during an acquisition (the modules are internally triggered), the logic analyzer designates the latest-occurring module trigger as the system trigger.

NOTE. *If an acquisition does not complete, due to one or more modules not receiving a trigger or not completing posttrigger acquisition, then you can manually stop the acquisition by clicking the Stop button. Clicking the Stop button effectively generates a system trigger and completes the acquisition.*

The system trigger is a latched event and it resets to a false state between acquisitions. The external system trigger input uses real-time gating and is only active (capable of latching system triggers) during the actual acquisition period.

The logic analyzer can also send an internally-generated system trigger out to the target system or to other test equipment through the SYSTEM TRIG OUT connector. All the external signal inputs and outputs operate at TTL levels. The connectors are located at the rear of the portable mainframe and at the front of the benchtop mainframe. For more information about external signaling capabilities, see *Intermodule and External Signaling* on page 3–41.

Arming Modules

Using the arm feature, you can use one module to control when another module accepts triggers. When module A arms module B, this means that module B does not begin looking for a trigger until it receives an arm signal.

Arming is accomplished through trigger actions. For the LA module, arming is specified in the Clause Definition dialog box; for the DSO module, arming is specified in the Trigger page. A module can arm any one of the other modules. The designated module can be armed by only one module. The same arming action can, however, appear multiple times within the same trigger program.

Arms are latched events which, once set, cannot be cleared until the acquisition is completed.

NOTE. *For a single module, arming and internal signaling are mutually exclusive. You cannot simultaneously arm modules and set signals. You can test for a set signal (for example, *If Signal X Is True*), but you must designate an external signal for this purpose; otherwise you will be unable to set the signal when using the arming feature.*

Intermodule and External Signaling

The logic analyzer has four internal signals that you can use to set up trigger conditions between modules, or to send or receive signals external to the logic analyzer. Use the Signals property page, shown in Figure 3–30, in conjunction with the module trigger programs to configure these signals for your application. The trigger programs determine when the signals occur. The Signals property page specifies characteristics of the signals.

NOTE. Be careful to observe the bandwidth and latency specifications when using internal and external signals. Refer to Tables A–19 and A–20 on pages A–18 and A–20 for information.

To open the Signals property page, go to the System menu and click System Configuration. Then select the Signals tab.

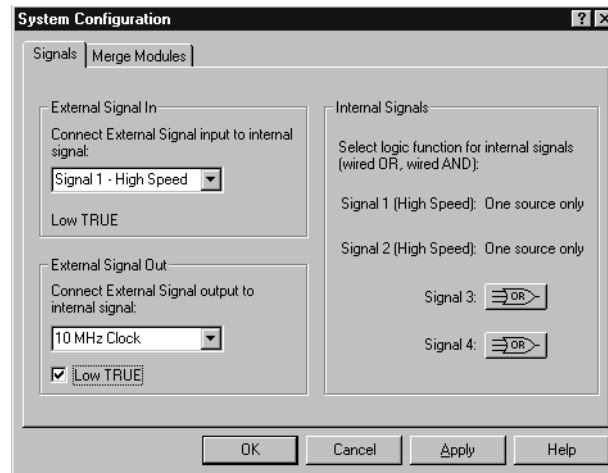


Figure 3–30: Signals property page

Only one module in the system can drive Signal 1 and only one module can drive Signal 2. When used with the expansion mainframe, all modules which drive Signal 3 should be in the same mainframe and all modules which drive Signal 4 should be in the same mainframe.

The logic analyzer and DSO modules use a logical expression (True/False) for Signals 1, 2, 3, and 4. However, the pattern generator module uses a physical expression (High/Low) for these signals. Please use the tables in *Appendix C: Pattern Generator Physical-Logical Conversion* to convert physical expressions to logical expressions or vice versa.

Internal Signals

All LA modules can set and clear any of the four internal signals. The DSO can set but not clear any signal. The logical output of these signals can be used as an event in other modules' trigger programs. You can also connect the internal signals to the External Signal In and External Signal Out connectors on the mainframe, so that you can use an external signal as a trigger event or send a signal out when a trigger condition is met.

Internal signaling is for users with special trigger programming requirements. Internal signaling adds flexibility to trigger programming, but also adds complexity. When using internal signaling you must take care that the signals are correctly set and cleared, and that the trigger programs for all modules are compatible with regard to signal usage. Also, you must have correctly set the internal signal attributes in the Signals property page.

Internal signaling is accomplished through trigger actions specified in the Clause Definition dialog box and the DSO Trigger page.

NOTE. *Arming and internal signaling are mutually exclusive. You cannot simultaneously arm modules and set signals. You can test for a set signal (for example, If Signal X Is True), but unless you have designated an external signal for this purpose, you will be unable to set the signal when using the arming feature.*

Signal Logic Function. To use internal signals, you must select which internal signal logic function is appropriate for your trigger program. Signals 1 and 2 (high speed) can be asserted by only one module each. For signals 3 and 4, the modules can be wired-OR or wired-AND. Selecting the OR function means that any module can assert the signal. Selecting AND means that all modules must set the signal for it to be asserted. The same logic applies to clearing signals.

The logic function applies only at a module level, not to multiple set/clear statements within a single module.

NOTE. *Be careful when using wired-AND internal signals. If your trigger depends on an internal signal, all modules must set the signal for it to be asserted, or the trigger will not occur. If you change your trigger program, remember to update the logic function settings accordingly.*

External Signals

The logic analyzer can send and receive signals to/from the target system using the External Signal In and External Signal Out connectors on the mainframe. Use the External Signal In function to include a signal from your target system as part of the trigger setup. Use the External Signal Out function to send a signal to the target system or other test equipment when a trigger condition is met.

The connection from the module to the external connector is made by one of the four internal signals. You must designate which internal signal is to be used for this purpose.

The external signal connectors are located at the rear of the portable mainframe and at the front of the benchtop mainframe. The external signals all operate at TTL logic levels.

Merging Modules

A merged LA module set consist of a master module and one or two slave modules. A merged pattern generator module consists of a master module and up to four slave modules.

LA Modules must have the same maximum state speed and must be physically connected in the mainframe before they can be merged by software. Modules must be adjacent and connected as described in *Appendix E: Merging Modules*.

Merged pattern generator modules are not physically connected in the mainframe but must be in adjacent slots in the same mainframe.

Modules that are capable of being merged, are shown in the Merge Modules property page with a merge button. See Figure 3–31.

To open the Merge Modules property page, go to the System menu and click System Configuration. Then select the Merge Modules tab.

To merge or unmerge modules, click the merge button between the module icons. You can unmerge the modules at any time for independent operation.

NOTE. After the LA modules have been physically merged, you should run the self-calibration procedure on the modules as a merged pair. To run the self-calibration procedure, go to the System menu and select Calibration and Diagnostics. Click Self Calibration.

Merged pattern generator modules do not need to be calibrated as a merged pair.

In setup and data windows, merged module probe names use the following convention: master module probe names are displayed normally, and slave

module probe names are prepended with an S. If you have more than two merged modules, the probe names are prepended with an additional number (such as S2).

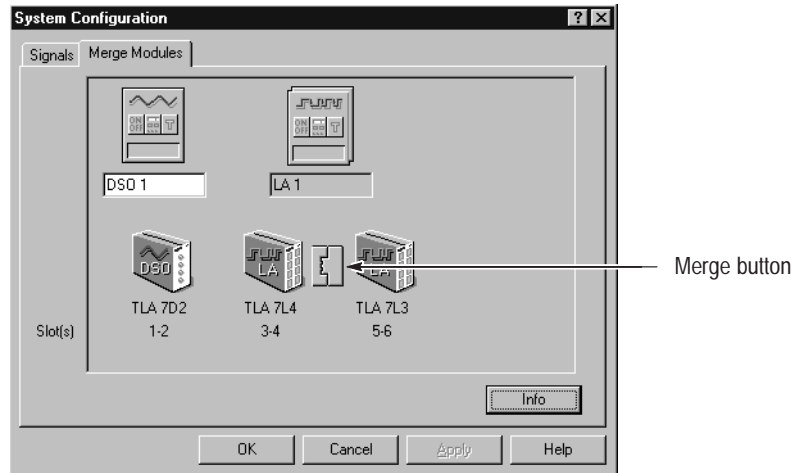


Figure 3–31: Merging modules

Saving and Loading Setups, Triggers, and Data

Once you set up the logic analyzer to your satisfaction, you will probably want to save the setup for future use. You can save setup information in two ways, a saved system file or a saved module file.

Refer to the *Logic Analyzer Conceptual Model* described on page 2–30. The modules consist of the setup, trigger, and data associated with the physical LA or DSO module installed in the logic analyzer. The system consists of the setup and data for the whole logic analyzer, including all the modules and all data windows. See Figure 3–32.

When you save a module, you save all the setup and trigger information for that module. When you save a system, you save all the setup information for the system, including data window display settings, and all the module information, as well. In either case, you have the option of saving acquired data.

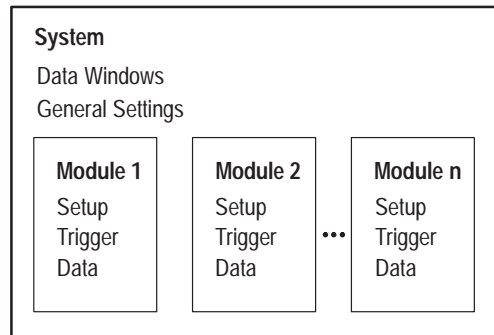


Figure 3-32: Logic analyzer conceptual model

Saving System and Module Files

Determine whether you want to save the information from a single module or for all modules. Select Save System or Save Module from the File menu.

In the Save As dialog box select one of the save options (see Figure 3-33):

- Select Save all Acquired Data to save setups and all data.
- Select Save only Unsuppressed Data to save the setups and unsuppressed data (only the data displayed in the Listing or Waveform window). Be aware that if you select this option, the suppressed samples are lost. If you want to save the suppressed samples select Save all Acquired Data.
- Select Don't Save Acquired Data to save the setups without any acquired data.

Saved system and module file names have a .tla file name extension (*file-name.tla*). The initial default location for saved files is C:\My Documents.

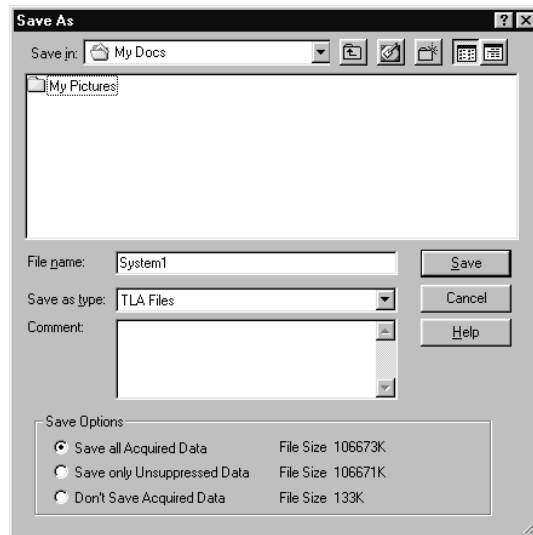


Figure 3–33: Saving a system with data

Loading Saved System and Module Files

The logic analyzer stores all the setup, trigger, and data information in just two types of files: saved module and saved system. However, the logic analyzer can extract different types of information individually from these files. From a saved module file, you have the option of loading any of the following:

- An LA module trigger program
- A module setup and trigger program
- Saved data from the module (accomplished by opening a saved data window; see *Opening a Saved Data Window* on page 3–59)

From a saved system file, you can load any of the following:

- Any of the previous module-related choices
- Full system setup, including data windows
- Saved data from one or more modules

You execute Load operations from the File menu. For module Load operations, you must first go to the module Setup or Trigger window before accessing the File menu.

Loading a System. When you load a system you load the full system setup, which includes setup, data, and trigger information for the logic analyzer and all installed modules. If the saved system file included data, the data windows and saved data are also loaded.

When you try to load a saved system with a different module configuration than your current system, the logic analyzer displays a dialog box (see Figure 3–34), giving you the option of using a suggested configuration. The suggested configuration is listed at the bottom of the dialog box. Click OK to accept the suggested configuration.

NOTE. *If you load a setup that you saved with suppressed samples, the suppressed samples are not present in the setup.*

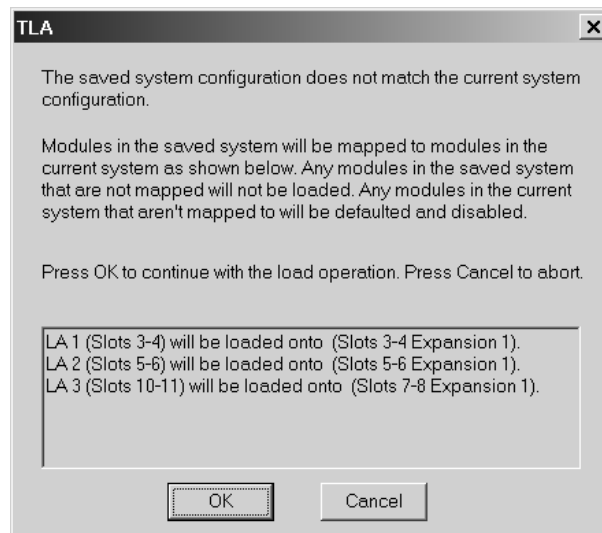


Figure 3–34: Loading a saved system that does not match the current system

If you click the Cancel button the logic analyzer displays the Load System Options dialog box. Use this dialog box to load specific modules from the saved system. To load a module from the saved system, drag the module icon from the top of the dialog box to a module icon in the bottom of the dialog box. Figure 3–35 shows an example of the Load System Options dialog box.

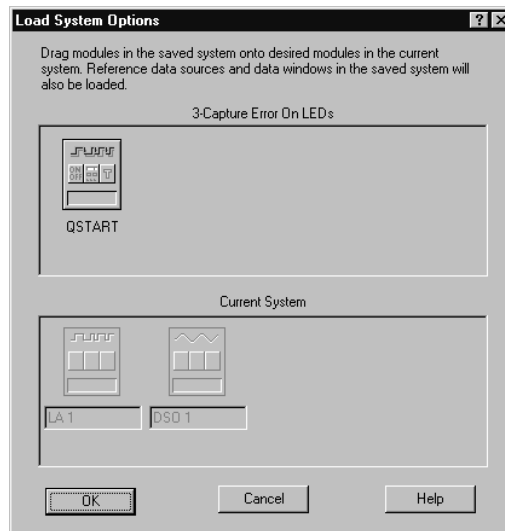


Figure 3–35: Load System Options dialog box

Loading a Setup and a Trigger Program. When you execute a Load System or Load Module operation, you load a saved setup and its related trigger program(s) to the logic analyzer (system) or specified module.

Loading Saved Data. You can load saved data using the Load Data Window selection in the Window menu. See *Opening a Saved Data Window* on page 3–59 for more information.

Loading a Saved Trigger. You can load an LA module trigger without loading a full setup. Saved system and module files contain trigger program information. When you load a trigger from the LA Trigger window, you can select a saved system or module file as the source. When you do so, the logic analyzer extracts only the trigger information from the file and loads it to the module.

Creating a Personalized Trigger Library. To create your own trigger library, follow these steps:

1. Create a folder in a convenient location.
2. Go to the Trigger window containing the trigger program you want to save.
3. Go to the File menu and select Save Module As.
4. In the Save As dialog box, navigate to your trigger library folder.
5. Name the new file, and use the Comment box to enter descriptive comments.

6. Make sure that Save Acquired Data is not selected.
7. Click Save.

Loading Default Settings

To return the logic analyzer to its default condition, go to the File menu and click Default System.

System Options

The logic analyzer provides several property pages where you can set or change system options. To access the system options, select Options from the System menu and choose the property page you are interested in.

- Use the Color property page to create, remove, and modify color schemes.
- Use the Defaults property page to specify the defaults throughout the application. The settings you enter will be the default settings when you create new data windows.
- Use the Preference property page to specify user preferences, such as changing the color of the Run or Stop buttons or hiding the Status bar.
- Use the Presets property page to view and modify preset names and values such as probe threshold voltages and DSO vertical range or vertical offset values.
- Use the Start-Up property page to select which system setup (such as a previous system or a saved system setup) to open after you power on the logic analyzer.
- Use the System Source Files property page to define the location of source files and suffixes used to create new Source windows.

Menu Shortcut Keys

You can use the shortcut keys listed in Table 3–5 to manipulate menus and edit windows. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

Table 3–5: Menu shortcut keys

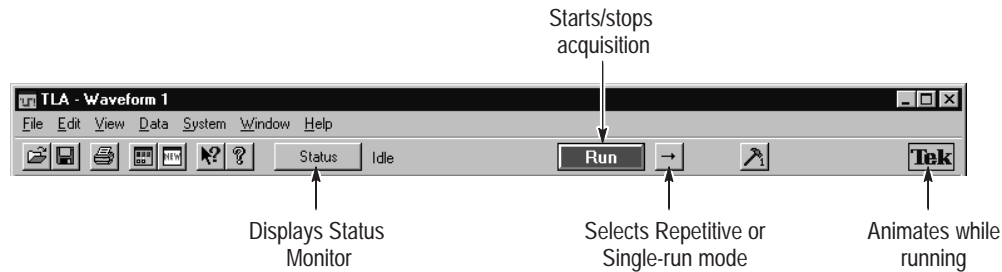
Desired action	Key combination
File menu	
Return system to the default setups	CTRL + D
Load a saved system	CTRL + O
Save a system setup	CTRL + S
Print the active window	CTRL + P
Edit menu	
Cut a selected item to the clipboard	CTRL + X
Copy a selected item to the clipboard	CTRL + C
Paste items from the clipboard	CTRL + V
Undo edit	CTRL + Z
Data menu	
Search backward	CTRL + B
Search forward	CTRL + F
System menu	
Display the Status Monitor	CTRL + M
Run or Stop	CTRL + R
Window menu	
Create a new data window	CTRL + N

Acquisition

When you start an acquisition, all modules start acquiring data together. (Exceptions are when one module has been programmed to arm another or when a module has been turned off.) Modules stop acquiring data individually, according to their trigger programming.

Starting and Stopping Acquisition

You control acquisition from the Control bar, shown below:



1. In the Control bar, click Run to start an acquisition.
2. The Tek icon on the right animates while the logic analyzer runs. Point at this icon with the mouse to display a tooltip showing the instrument status.
3. Wait for the logic analyzer to trigger and display data, or click Stop to manually stop an acquisition.

There are two ways to acquire data: Single-run or Repetitive mode. Within Repetitive mode, you can specify the following three conditions:

- Save Module and Data
- Stop if Compare with Reference is Equal or Not Equal
- Stop After N Acquisitions

When comparing acquisition data against reference data, you can view the results in either a Listing window or in a Waveform window.

Single Run Mode

In Single-run mode, the logic analyzer automatically stops acquiring and displays data when it fulfills the setup conditions. Use Single-run mode to find and display a specific event.

During acquisition, the logic analyzer monitors the data, looking for the events you specified in the Trigger windows. When the specified events occur, the logic analyzer responds according to the selections you made in the Setup and Trigger windows.

Repetitive Mode

In Repetitive mode, the logic analyzer keeps acquiring data until you click Stop or until it fulfills the stop conditions.

You can use Repetitive mode as follows:

- To observe the same waveform or listing for a period of time
- To stop after a set number of acquisitions for a period of time and look for differences

After each acquisition you can have the logic analyzer do the following tasks:

- Save the system or module setups and data
- Export the data to separate files or overwrite the same file
- Compare the acquisition data against data in another LA module or a saved LA module file
- To open a file or execute a set of defined tasks after the acquisition is complete. For example, you can execute command such as sending email or paging you that the logic analyzer has stopped.

Select Repetitive Properties from the System menu to select the different options for the Repetitive mode. Figure 3–36 shows an example of the Repetitive Properties dialog box.

NOTE. You can minimize the time between acquisitions by specifying compare conditions under the LA Setup window, deleting (not just minimizing) all data windows, and then starting the logic analyzer. When the logic analyzer fulfills the compare conditions, you can create a new data window with the New Data Window wizard to view the data.

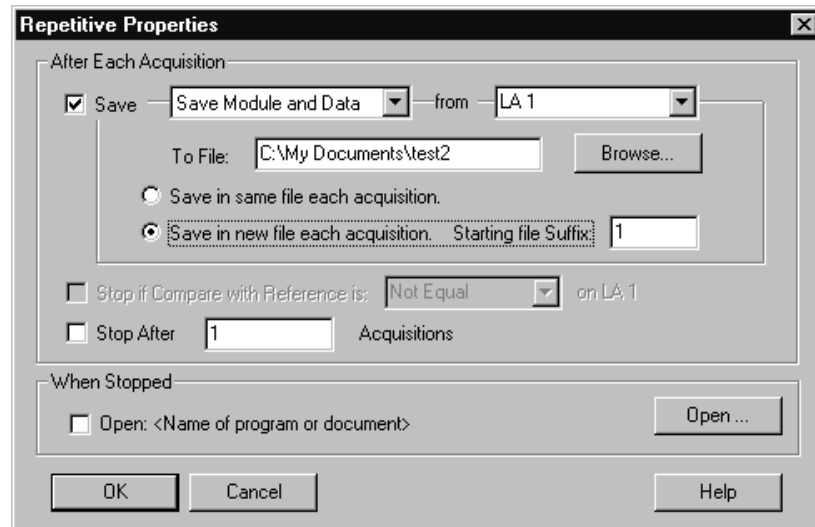


Figure 3–36: Defining setups for Repetitive mode

Viewing Acquisition Activity

While the logic analyzer is acquiring data, you can check its progress to see how much data it has acquired or to view channel activity.

Use the Status Monitor for a brief summary of acquisition, trigger, and data storage progress. See Figure 3–37.

To display the Status Monitor click Status on the Control bar.

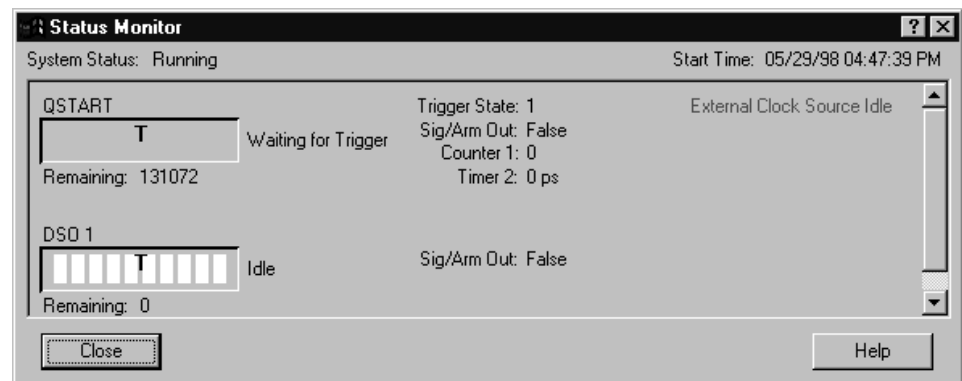


Figure 3–37: The Status Monitor

The Status Monitor is also useful to debug a trigger program. From the Status Monitor you can view the current status of various resources of the logic analyzer during acquisition. Be aware that rapid changes in trigger state, counter values, timer values, and the internal signals cannot be accurately displayed in real time in the Status Monitor.

If the Logic Analyzer Does Not Trigger

If the logic analyzer does not trigger, then you should check the following:

- Check that your target system is powered on.
- Check the System window to verify that required modules are turned on.
- If the module has correctly clocked data, acquired the specified events, triggered, but has not stopped, the module probably has not acquired enough additional data to fill acquisition memory. Click Stop to manually stop the acquisition, and then change the module Memory Depth (reduce) or Trigger Position (increase).

LA Module

The following conditions apply to the LA module only:

- Check the Status Monitor for an external clock warning. If the LA is not receiving an external clock, the Status Monitor displays the following message: External Clock Source Idle.
- Check for signal activity at the probe tip. If there is no activity, then check the probe connections.

Check the clock signal to make sure that the LA module is actually clocking data. Problems with the clock signal can impact setups using external clocking, custom clocking (microprocessor support packages only), or storage qualification.

- Similar to the previous item, check clock qualifier signals and clocking equations.
- Check the threshold voltages for probes and clocks.
- If the module is correctly clocking data and the data events have occurred, but the trigger program did not generate a trigger, then you should check the trigger program itself. The trigger program might not be reaching the state that generates the trigger. Use the Status Monitor to track trigger program progress and identify the state in which trigger progress stops.

- Check the complexity of your trigger program. If your trigger program is too narrowly defined, or over-specified, the trigger program might not acquire the desired data or might not trigger. A less-specific trigger program might acquire the desired data and will also verify that you have set up the proper clocking and threshold levels.

DSO Module

The following condition applies to the DSO module only:

- Check the trigger Mode setting. If Mode is set to Normal, and the data does not meet the trigger conditions, the module will not trigger. (Conversely, if Mode is set to Auto, the module will trigger after a set length of time, even if the specified data does not occur.)

Arming or Intermodule Triggering

The following conditions apply only if you are using arming or intermodule triggering:

- Internal signal logic function. If your trigger depends on setting an internal signal, and that signal has been set to Wired-And, all modules in the system must set the signal or it cannot assert.
- If any modules are turned off, check that the trigger program is not waiting for input from an inactive module.

First Transition Indication Problems

Because the logic analyzer does not clear the first transition indication, check that the LA modules always show a first transition indication (even if there are no probes attached).

To avoid triggering on a false first transition indication, set the first state to “If Anything, Go to Next State.” This will use a state, but it ensures that you do not trigger on a false transition indication.

Display

To view acquired data, open one of the data windows. The Listing window and the Waveform window are the data windows that you will use for most applications; see Figure 3–38. You can also create Source windows to use with high-level language support applications or Histogram windows to use with performance analysis applications. You can have multiple data windows to display different data or different views of the same data.

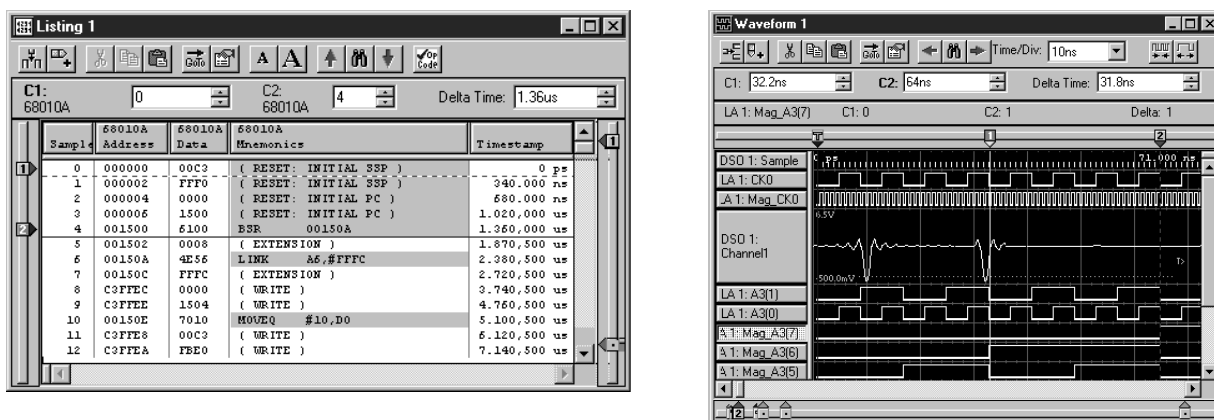


Figure 3–38: The Listing and Waveform windows

Setup window and data window controls act independently of one another. Controls in the Setup windows affect how the modules acquire data. Controls in the data windows affect how the acquired data is displayed.

NOTE. LA Listing and Waveform windows are different from pattern generator Listing and Waveform windows. LA Listing and Waveform windows display acquired data from the target system while pattern generator Listing and Waveform windows are used to set up data to send to the target system.

Opening an Existing Data Window

The System window shows the relationship between the modules and the data windows.

- To open a data window, go to the System window and click a data window button. See Figure 3–39.
- To see which modules supply data to a data window, go to the System window and click the data window label.

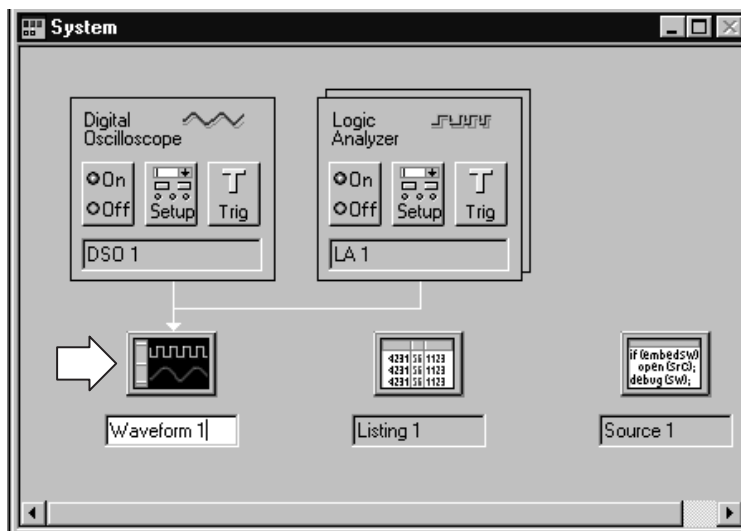


Figure 3–39: Opening a data window

Opening a Saved Data Window

To open a window displaying data from a saved system file, do the following:

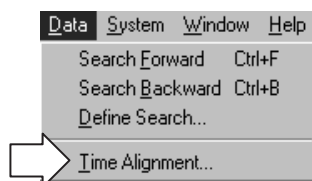
1. Go to the Window menu and select Load Data Window.
2. Click Browse to search for the file or enter a path to the file in the text box.

NOTE. The saved file must be a saved system file.

3. Once the file is found, click Open.
4. Select the data window to load.
5. Click OK.
6. If the data window name is not unique, you will be prompted for a new name. Enter a name and click OK.

Aligning Saved Data with Current Data

Saved data and current data are time-correlated by aligning their system triggers. You can manually adjust this alignment using the Time Alignment dialog box. To access the Time Alignment dialog box, go to the Data menu and select Time Alignment, as shown below.



Creating a New Data Window

Use the New Data Window wizard to create a new data window for the data you want to display. You can select data from any module, a saved system file, or saved module file. See Figure 3–40.

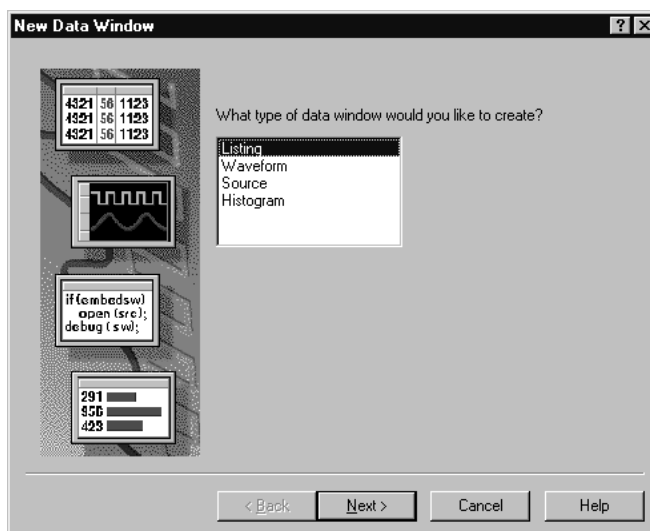


Figure 3–40: New Data Window wizard

Create a new data window as follows:

1. Click the New Data Window icon in the toolbar.
2. Select the appropriate Window Type and click Next.

NOTE. The contents of the New Data Window wizard will vary depending on the type of data window that you are creating.

3. For each page in the wizard, enter the required information and click Next.
4. On the last page, enter the name for the data window or use the default name and then click Finish.

General Purpose Data Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–6 to move data and cursors in data windows. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- Arrow keys with the Control (CTRL) key move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3–6: General purpose data window shortcut keys

Desired action	Key combination
Scroll data up 10 pages	Shift + Page Up
Scroll data down 10 pages	Shift + Page Down
Scroll data to the top of the window	Shift + Home
Scroll data to the end of the window	Shift + End
Move active cursor up one page	CTRL + Page Up
Move active cursor down one page	CTRL + Page Down
Move active cursor to the top of the data	CTRL + Home
Move active cursor to the end of the data	CTRL + End
Move active cursor up 10 pages	CTRL + Shift + Page Up
Move active cursor down 10 pages	CTRL + Shift + Page Down
Move active cursor to the top of the data	CTRL + Shift + Home
Move active cursor to the end of the data	CTRL + Shift + End

Waveform Window

Use the LA or DSO Waveform window to display and evaluate acquisition data. You can display both DSO waveforms and LA waveforms simultaneously. Each window contains a data area, waveform labels, marks and several tool bars that allow you to measure and manipulate your waveforms. See Figure 3–41 for an example.

For the LA module, data values for each channel are shown as a digital (two-state) waveform. Logic level low is drawn as a thick line; logic high as a thin line. For the DSO module, data values for each channel are displayed as an analog waveform.

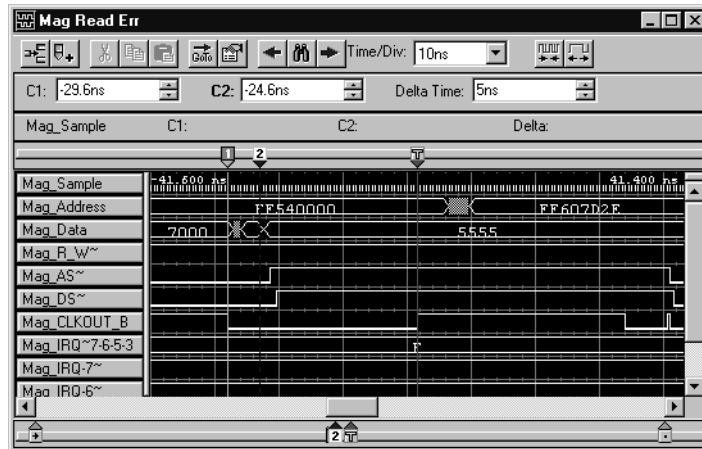


Figure 3–41: Waveform window

Types of Waveforms

There are several types of waveforms that can be shown in the Waveform window, as shown in Figure 3–42.

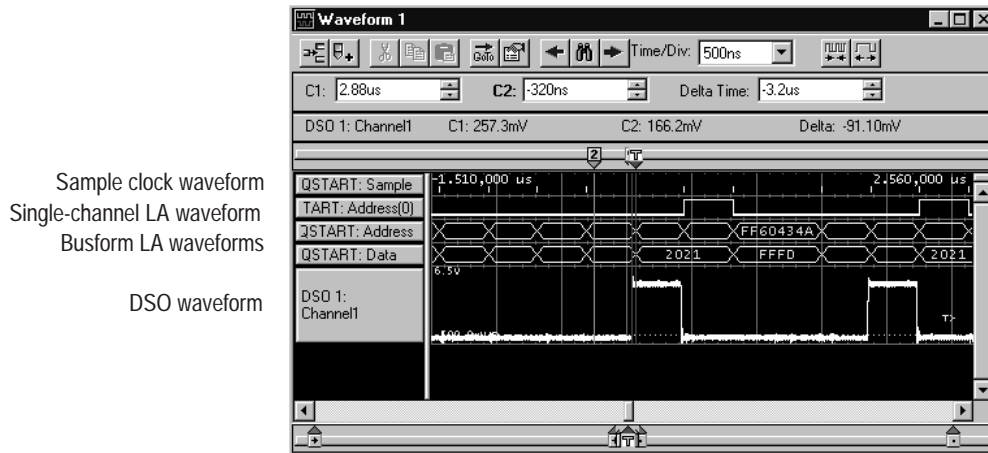


Figure 3–42: Waveform types

Sample Clock Waveforms

Each module that contributes current data to the window has its own sample clock waveform. The sample clock waveform consists of a row of short vertical tick marks placed along the time axis at each display point that represents an actual acquired sample for the module.

Single-Channel LA Waveforms

Digital timing diagrams that represent a single LA channel.

Busforms

Busforms display the value of an LA module channel group.

Magnitude Waveforms

Magnitude waveforms plot the numeric value of a channel group on a vertical axis over a period of time. For example, you can use magnitude waveforms with A/D and D/A applications for viewing the RGB components of a digitized video signal. Figure 3–43 shows such a component.

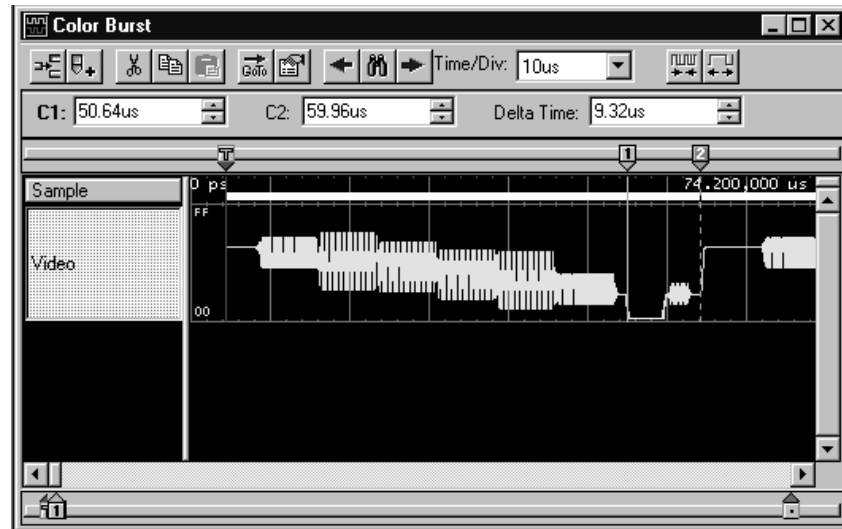


Figure 3–43: Magnitude waveform

DSO Waveforms

DSO waveforms are analog timing diagrams that represent a single DSO channel.

The size of the DSO waveform depends on signal size and the input voltage range selected in the DSO Setup Window.

Range readouts for DSO waveforms are located at top and bottom left of the waveform. The range readouts show the maximum and minimum vertical input voltage settings for the waveform. See Figure 3–44.

The ground line appears as a horizontal dotted line through each DSO waveform. If ground is outside the bounds of the waveform, the line is not shown.

The trigger threshold is indicated by a “T>” at the right side of the waveform. Set the trigger threshold in the Trigger page of the DSO Setup window.

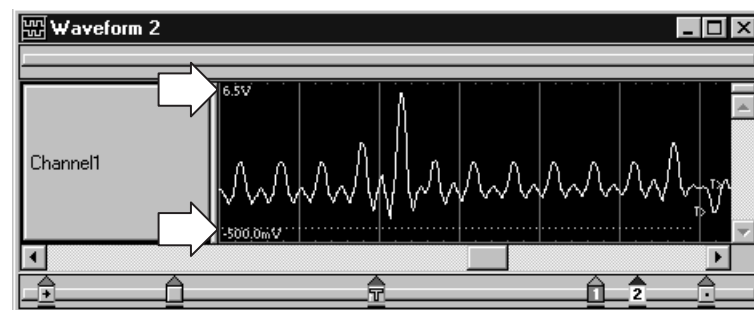


Figure 3–44: Range readouts

Reading the Waveform Indicators

Data marks, cursors, and other indicators help you navigate and identify the data. Figure 3–45 and Table 3–7 identify and describe data window marks.

To move cursors or marks, drag the cursor and mark handles. Trigger marks and Begin/End data marks cannot be moved. For more information on using marks, refer to the online help.

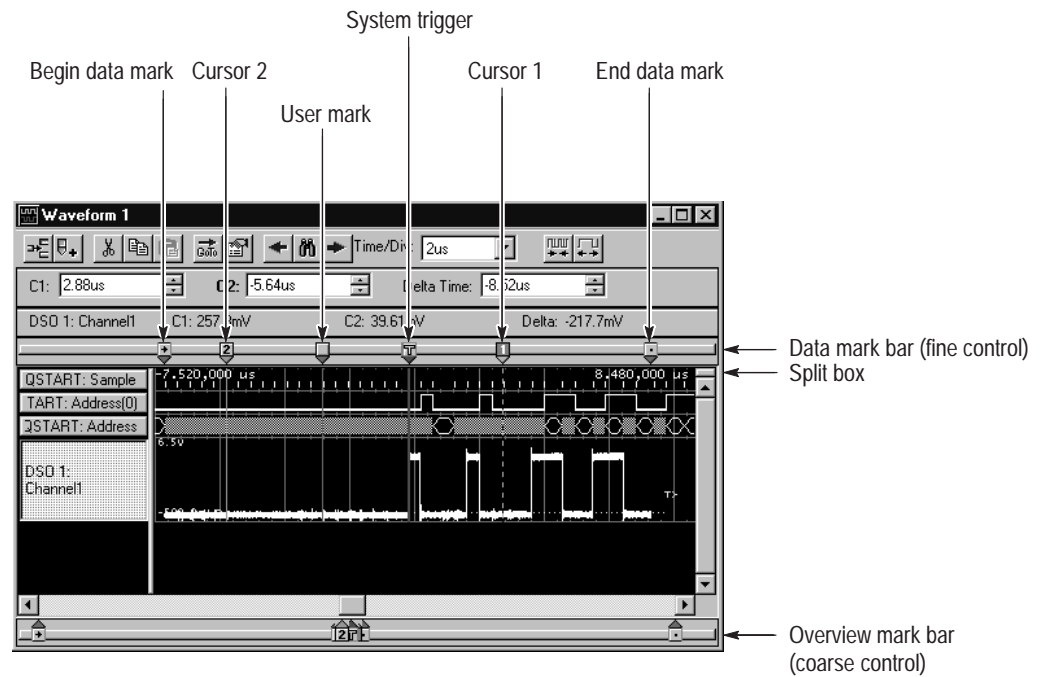







Figure 3–45: Waveform window cursors and marks

Table 3–7: Waveform window cursor and mark summary

Mark	Name	Description
	System trigger	The system trigger is the reference point for the acquisition. Timing and location information is relative to the system trigger. Trigger marks cannot be moved. Under some conditions the system trigger associated with a module's data might not be displayed in the data window. If the system trigger was caused by another module, whose data is not included in the current display, then the system trigger is not shown. Nevertheless, all time measurements still relate to that system trigger, even if it is not shown. The system trigger associated with the current data is called the active system trigger. The system trigger associated with saved data is called the reference system trigger. The active system trigger is indicated by a yellow T; the reference system trigger is indicated by a gray T.
	Module trigger	The point at which the module triggered. Trigger marks cannot be moved.
	Begin data / end data	The start and end of a module's data record. These data marks cannot be moved.
	Cursors 1 and 2	Moveable marks used for visual reference and for data measurements.
	User mark	User-created marks. Use marks to make specific data more easy to identify and find.

Zoom Box

Use the Zoom box feature (see Figure 3–46) to zoom on waveform details with a click and drag of the mouse.

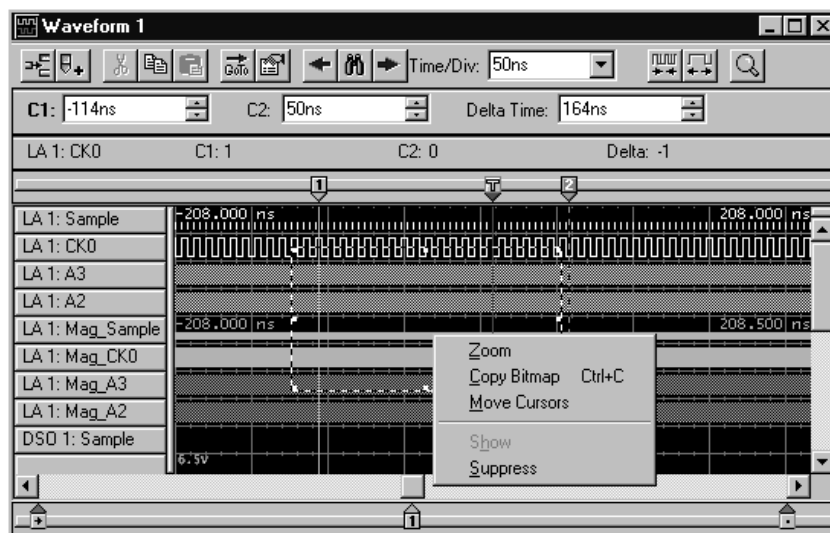


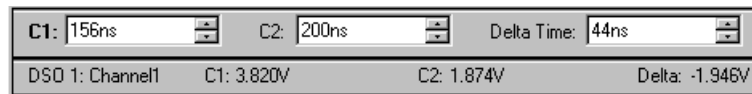
Figure 3–46: Waveform window zoom box

Point to the area of interest on the screen, click the left mouse button, and drag the cursor to create a zoom box. After you create the box, right click the mouse to display a menu containing several options.

- Select Zoom from the menu to zoom on the area of interest.
- Select Copy Bitmap to copy the area inside the zoom box to the clipboard. You can then use tools such as MS-Paint to edit the bitmap for use in different applications.
- Select Move Cursors to move the cursors to both sides of the zoom box. You can then easily make cursor measurements from the new cursor positions.
- Select Suppress to suppress or hide the waveforms under the boundaries of the zoom box. To unsuppress the waveforms, right-click the mouse, select Define Suppression, and select Show All acquired samples in the dialog box. Click OK to close the dialog box and the suppressed samples are restored.

Taking Cursor Measurements

Use the cursors to take time and voltage measurements. You take time and voltage measurements in the Waveform window, as shown below.



The following steps describe how to take a time measurement. (Magnitude on an LA module waveform is expressed as a 1 or a 0.)

1. In the Waveform window, select a waveform.
2. Move Cursor 1 to the location on the waveform that you want to measure.
3. Read the time from the C1 readout on the measurement bar.
4. Move Cursor 2 to another location on the waveform that you want to measure.
5. Read the time from the C2 readout on the measurement bar.
6. Read the time difference between the two waveform locations from the Delta readout on the measurement bar.

The Delta readout is not an absolute delta because the delta can be either positive or negative. For example if you place Cursor 2 before Cursor 1, the result will be a negative value. Cursor time is relative to the active system trigger.

Jumping to Specific Data Locations

You can use the Go To dialog box to jump to a new position by selecting any current mark or waveform. To open the Go To dialog box, open a Waveform window and click the Go To tool bar button, as shown in Figure 3–47.

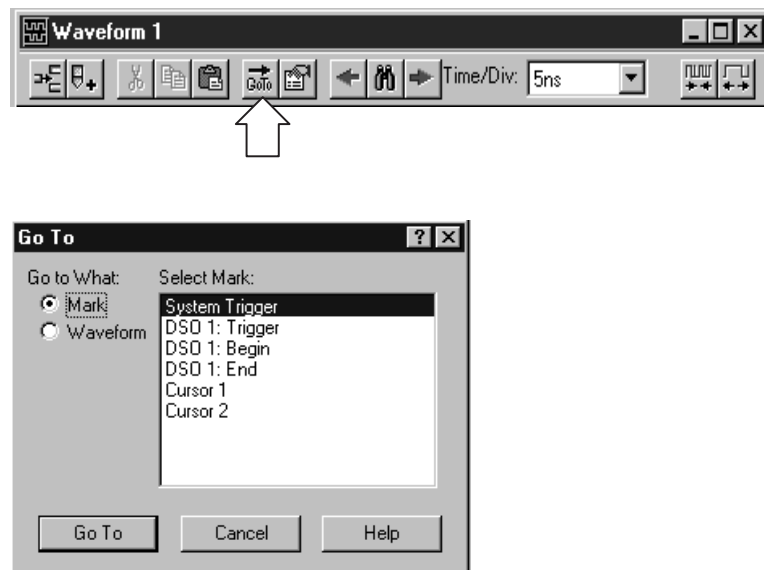


Figure 3–47: Using the Go To dialog box to jump to the system trigger

You can also use the Overview Mark bar to jump to another location. If you do not click on a mark, clicking in the Overview Mark bar scrolls to that location.

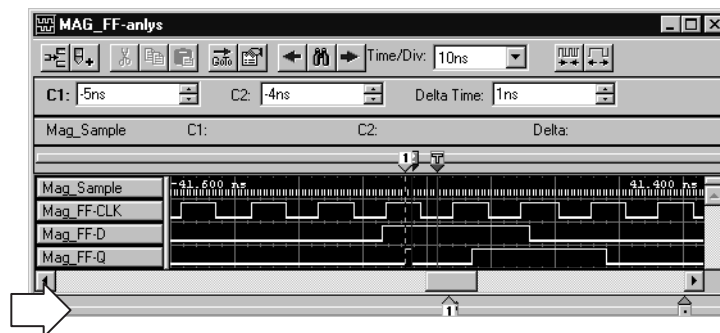
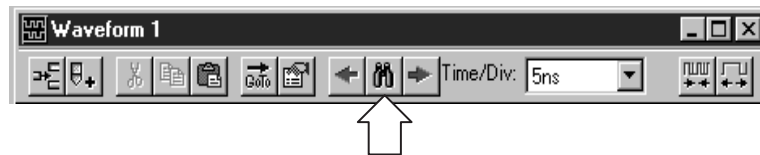


Figure 3–48: Using the Overview Mark bar to jump to a data location

Searching Data

Use the Define Search dialog box (see Figure 3–49) to search for specific data within the current Waveform window. Searches are specific to the selected data source and begin from the active cursor.

Click on the search icon to open the dialog box and fill out the search conditions. Cursor 1 marks the first occurrence of the item you searched for.



You can search any data source available to the current data window, but you can only search one data source at a time. For additional searches of the same event, click the Search Forward and Search Back arrow buttons in the tool bar (on either side of the search icon).

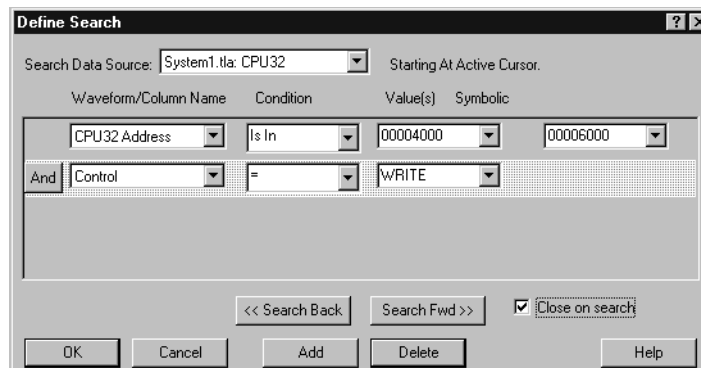


Figure 3–49: Defining search criteria

Hidden data or suppressed samples cannot be found by the search function. For example, if you turn off a waveform in the Waveform property page by deselecting Show Waveform, the search function cannot search for that waveform data.

Figure 3–50 shows a waveform window with suppressed samples (indicated by the hidden samples). If you try search for suppressed data, the instrument will skip over the suppressed area and search for visible data. If the suppressed data is still in memory, you can unsuppress the data (right-click the mouse, select Define Suppression, select Show All acquired samples in the dialog box, and then click OK to close the dialog box). You can then search for the data.

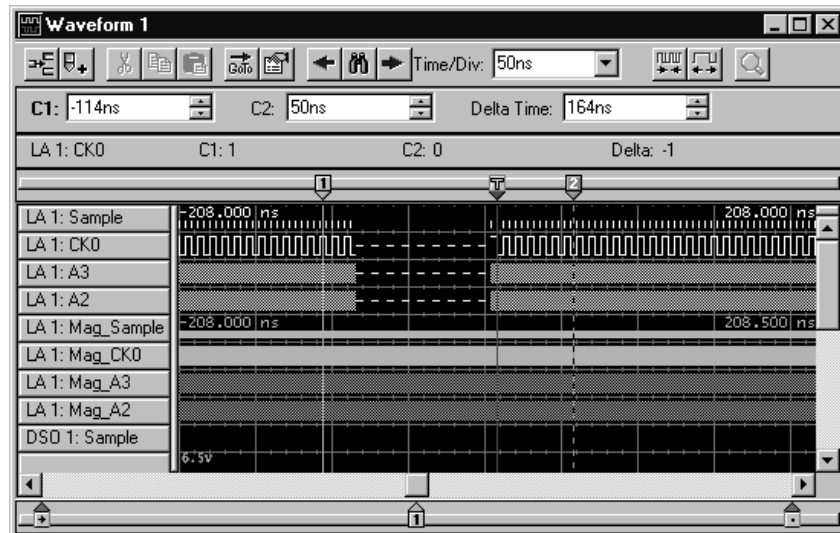


Figure 3–50: Suppressed samples in a Waveform window

Be aware, however, that you cannot unsuppress samples from a saved setup where you selected Save only Unsuppressed Data in the Save As dialog box.

Locking Windows

Locking windows provides an easy method to compare data from two different windows. Use the Lock Windows dialog box, shown in Figure 3–51, to select how windows are locked together.

To open the Lock Windows dialog box, go the System window and click the button for the data window you want to open. Go to the View menu and select Lock Windows.

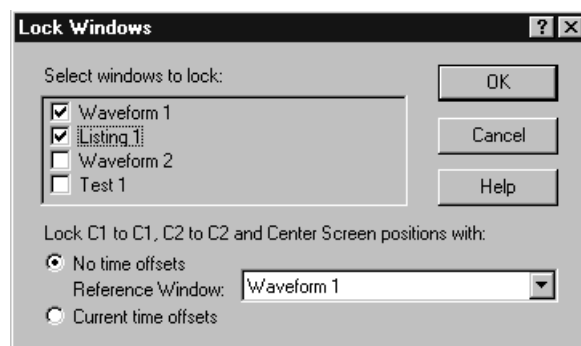


Figure 3–51: Lock Windows dialog box

MagniVu Data

The LA modules have MagniVu data acquisition as a standard feature. MagniVu data acquisition offers 500 picosecond, high-speed timing simultaneous with 100 or MHz 200 MHz state on all channels through the same probe; no double probing is required. The record length for MagniVu data is 2000 samples. MagniVu data is centered on the LA module trigger. Figure 3–52 shows an example of MagniVu data.

You can view MagniVu data in both Listing and Waveform windows.

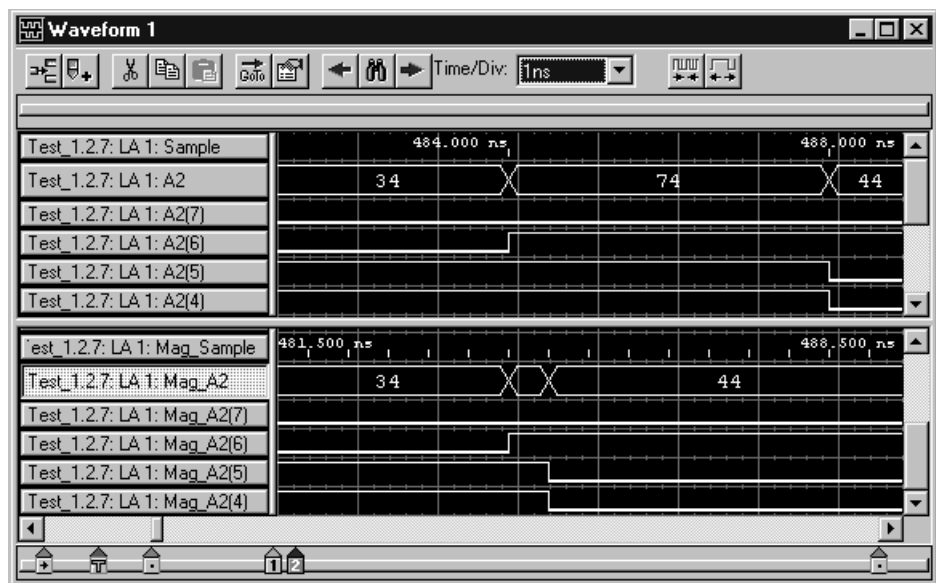


Figure 3–52: MagniVu data

In Figure 3–52, the top waveforms were acquired at the fastest normal sample rate. The MagniVu waveforms, in the lower part of the display, were acquired through the same probe channels at the same time as the top waveforms.

Take a close look at the difference in the acquired data. First view the regular data acquisition, which was sampled at 4 ns. The regular acquisition captured the address bus as it made the transition from 34 to 44. The data shows an invalid address of 74, and indicates that the invalid address lasts for the entire 4 ns sample period. At the next sample, the address is shown correctly as 44.

Now view the MagniVu data acquisition, which was sampled at 500 ps. The MagniVu data shows the same address bus transition from 34 to the invalid address of 74, before settling to the correct address of 44. Note, however, that the indicated settling time is different. The MagniVu data shows that the address bus took approximately 500 ps to complete the transition, and shows the address bus as 44 approximately 3.5 ns earlier than did the regular acquisition data.

Comparing Waveform Data

When comparing data against reference data, you can highlight data that is equal to or not equal to the reference data.

NOTE. Before you can display compare data, you must define the compare parameters in the Define Compare Dialog box in the LA Setup window. Refer to Memory Compare beginning on page 3–5 for information on setting up the compare parameters.

The following steps describe how to display compare data in the Waveform window.

1. Open a Waveform window and click the Properties tool bar button, as shown.



2. Select the Waveform Window property page.
3. Select Show Compare and select one of the colors for when data does not equal the reference data (Acq!=Ref).

If you want to highlight data that does equal the reference data, select Acq=Ref and the appropriate color (see Figure 3–53).

4. Click OK.

The data differences or equalities will be highlighted in the Waveform window in colors you specified.

NOTE. For more information on comparing data, refer to Guidelines for Memory Compare on page 3–7.

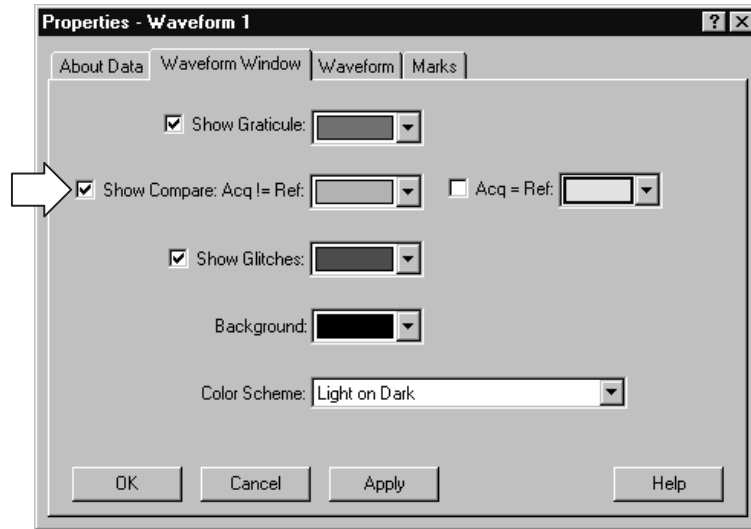


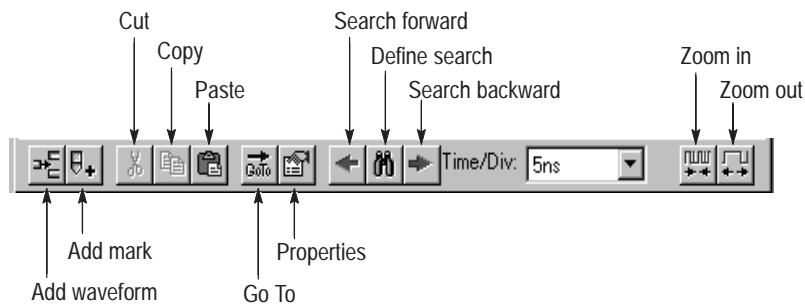
Figure 3–53: Selecting compare data colors in the Waveform Window property page

Adjusting the Waveform Data View

There are a number of actions you can perform in the Waveform window to get the exact view of the data that you want.

Waveform Window Tool bar

The tool bar has shortcut buttons for common operations, as shown below:



Moving Waveforms

Select the waveform labels and then drag them to their new location.

Adding a New Waveform or a Data Source

Click the tool bar Add Waveform button to open the Add Waveform dialog box. Then select the data source and its associated group or channel to add it to the display.

To select a group, first select By Group. (See Figure 3–54.) Then, from the list, select a group name indicated by a the + symbol. Default groups are displayed as busforms. (You can also choose to display a group as a magnitude waveform. Double-click the waveform label. From the waveform properties page, click Options and select Magnitude.)

To select individual channels, first select By Probe. Then, from the list, select the channel(s). If you have named individual channels in the LA Setup window, you can select By Name to list just those channels.

If the data source you want is not listed, click Add Data Source and find and select the source. (The data source can be an installed module or a saved module file.) See Figure 3–54.

New waveforms are added after the selected waveforms or after all waveforms if none are selected.

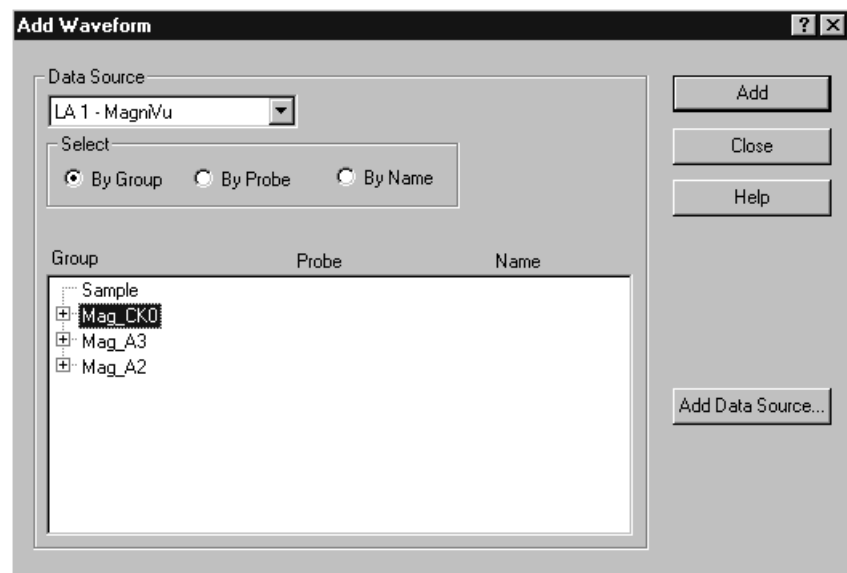


Figure 3–54: Add Waveform dialog box

Deleting Waveforms

Select the waveform labels, then click the Cut button on the tool bar.

Changing Waveform Label Width

To change the width of a waveform label, select and drag the waveform label border.

Changing Waveform Height

To change the height of a waveform, double-click on the waveform label to open the Waveform property page. Enter a new value or use the spinbox controls to change the value in the Height box.

In addition to adjusting the height using the Waveform property page, you can select the waveform, and adjust the waveform from the front-panel Size control on the portable mainframe.

Changing the Displayed Time/Div

Change the displayed time per division using the Time/Div tool bar control. You can also use the Zoom In and Zoom Out tool bar buttons.

Cut, Copy, and Paste

You can cut, copy, and paste waveforms and marks.

Viewing Glitches

Glitches are indicated on a waveform by a block of color behind the waveform. See Figure 3–55. Turn the glitch display on or off from the Waveform window property page.

NOTE. To view glitches in a data window, you must enable Glitch storage in the LA Setup window before acquiring data.

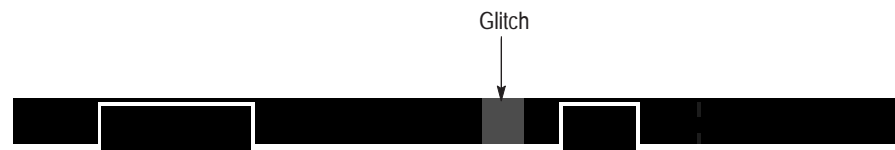


Figure 3–55: Waveform with a glitch

Naming Waveforms

Rename a waveform by returning to the Setup window and changing the channel or channel group name.

Splitting the Data Area

You can split the data area to compare waveforms that are far away from each other within the display. Drag the split box from the top end of the vertical scroll bar.

Customizing the Waveform Window Data

Use property sheets to customize data windows. Property sheets control aspects of the display such as size, color, and in some cases, enabling or disabling whether an element is shown. Click the Properties tool bar button in the Waveform window to open the data window property sheet. Figure 3–56 shows a property page.

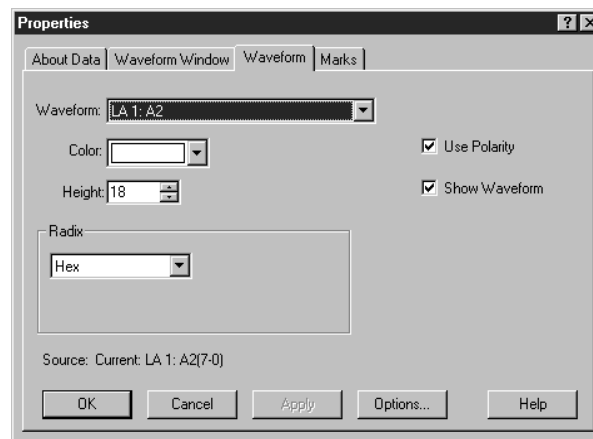


Figure 3–56: Property page

Exporting Waveform Data

You cannot export waveform data directly. However, you can add DSO waveform information as a column in a Listing window and then export the data as a listing file.

Refer to *Exporting Listing Data* on page 3–90 or more information on exporting data.

Waveform Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–8 to move data and cursors in the Waveform window. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- Arrow keys with the Control (CTRL) key move the active cursor.
- The Shift key increases movement by a factor of 10.

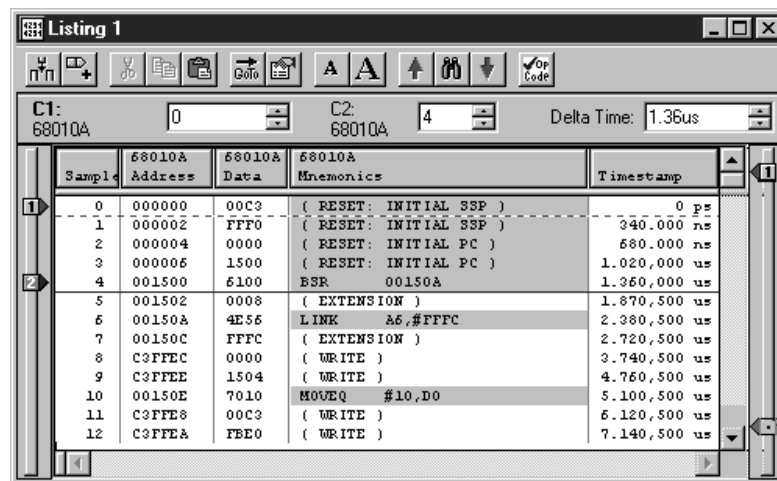
Table 3–8: Waveform window shortcut keys

Desired action	Key combination
Go to next trigger	CTRL + T
Display Go To dialog box	CTRL + G
Move Cursor 1 to the center of the window	CTRL + 1
Move Cursor 2 to the center of the window	CTRL + 2
Zoom in	CTRL + I
Zoom out	CTRL + U
Add a mark	CTRL + K
Add a waveform	CTRL + W
Scroll data left 50 pixels	Shift + Left arrow
Scroll data right 50 pixels	Shift + Right arrow
Move active cursor left five pixels	CTRL + Left arrow
Move active cursor right five pixels	CTRL + Right arrow
Move active cursor left 50 pixels	CTRL + Shift + Left arrow
Move active cursor right 50 pixels	CTRL + Shift + Right arrow

Listing Window

Use the LA Listing window to view and evaluate acquisition data. Data is presented as tabular text in columns that represent channel groups. Other columns are sample numbers and time stamp values. See Figure 3–57 for an example.

This window displays the amount of data you specified in Setup and Trigger windows. Each row in the table consists of data sampled on one acquisition cycle, and is assigned a sample number. Sample numbers are relative to the beginning of memory.



The screenshot shows a window titled "Listing 1" with a toolbar and configuration fields. The configuration fields show C1: 68010A, C2: 68010A, and Delta Time: 1.36us. The table below contains the following data:

Sample	68010A Address	68010A Data	68010A Mnemonics	Timestamp
0	000000	00C3	(RESET: INITIAL SSP)	0 ps
1	000002	FFFO	(RESET: INITIAL SSP)	340,000 ns
2	000004	0000	(RESET: INITIAL PC)	680,000 ns
3	000006	1500	(RESET: INITIAL PC)	1,020,000 ns
4	001500	6100	BSR 00150A	1,360,000 ns
5	001502	0008	(EXTENSION)	1,870,500 ns
6	00150A	4E56	LINK A6,#FFFC	2,380,500 ns
7	00150C	FFFC	(EXTENSION)	2,720,500 ns
8	C3FFE0	0000	(WRITE)	3,740,500 ns
9	C3FFE4	1504	(WRITE)	4,760,500 ns
10	00150E	7010	MOVEQ #10,D0	5,100,500 ns
11	C3FFE8	00C3	(WRITE)	6,120,500 ns
12	C3FFEA	FBE0	(WRITE)	7,140,500 ns

Figure 3–57: Listing window

Reading the Listing Window Indicators

Data marks, cursors, and other indicators help you navigate and identify the data. Figure 3–58 and Table 3–9 identify and describe data window marks.

To move cursors or marks, drag the cursor and mark handles. Trigger marks and Begin/End data marks cannot be moved.

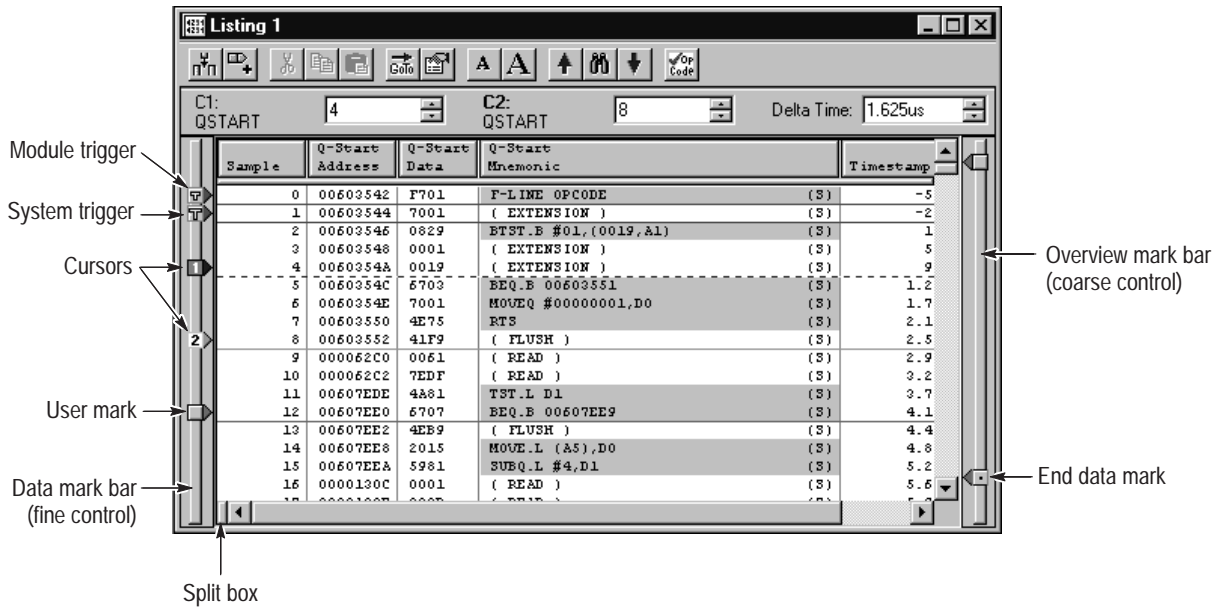


Figure 3–58: Listing window cursors and marks

Table 3–9: Listing window cursor and mark summary

Mark	Name	Description
	System trigger	The system trigger is the reference point for the acquisition. Timing and location information is relative to the system trigger. Trigger marks cannot be moved. Under some conditions the system trigger associated with a module's data might not be displayed in the data window. If the system trigger was caused by another module, whose data is not included in the current display, then the system trigger is not shown. Nevertheless, all time measurements still relate to that system trigger, even if it is not shown. The system trigger associated with the current data is called the active system trigger. The system trigger associated with saved data is called the reference system trigger. The active system trigger is indicated by a yellow T; the reference system trigger is indicated by a gray T.
	Module trigger	The point at which the module triggered. Trigger marks cannot be moved.
	Begin data / end data	The start and end of a module's data record. These data marks cannot be moved.
	Cursors 1 and 2	Moveable marks used for visual reference and for data measurements.
	User mark	User-created marks. Use marks to make specific data more easy to identify and find.

Taking Cursor Measurements

Use the cursors to take time measurements. Take time measurements in the Listing window, as shown below.



1. In the Listing window, move Cursor 1 to the location that you want to measure.
2. Read the time from the C1 readout on the measurement bar. Cursor time is relative to the active system trigger.
3. Move Cursor 2 to another location that you want to measure.
4. Read the time from the C2 readout on the measurement bar.
5. Read the time difference between the two locations from the Delta readout on the measurement bar.

Jumping to Specific Data Locations

You can use the Go To dialog box to jump to a new position by selecting any current mark or waveform. To open the Go To dialog box, open a data window and click the Go To tool bar button as shown in Figure 3–59.

You can also use the Overview Mark bar (see Figure 3–60) to jump to another location. If you do not click on a mark, clicking in the Overview Mark bar scrolls to that location.

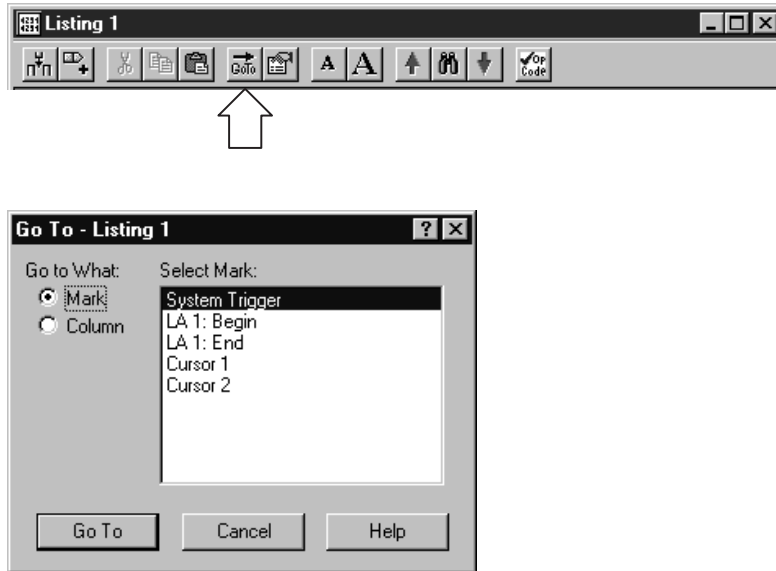


Figure 3-59: Using the Go To dialog box to jump to the system trigger

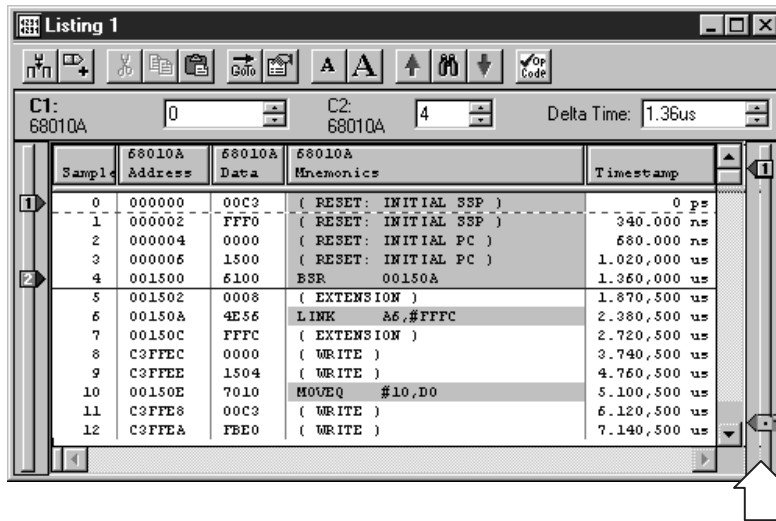


Figure 3-60: Using the Overview Mark bar to jump to a data location

Searching Data

Use the Define Search dialog box (see Figure 3–61) to search for specific data within the current Listing window. Searches are specific to the selected data source and begin from the active cursor.

Click on the search icon to open the dialog box and then fill out the search conditions. Cursor 1 marks the first occurrence of the item you searched for.



You can search any data source available to the current data window, but you can only search one data source at a time. For additional searches of the same event, click the Search Forward and Search Back arrow buttons in the tool bar.

Hidden data cannot be found by the search function. For example, if you turn off a column display in the Column properties page by deselecting Show Column, you cannot search for data in that column. Similarly, suppressed data can not be found by the search function; suppressed data in the listing window can be identified by gaps in sequence numbers.

You can unsuppress data and then use the search function as long as the data is in memory. However, you cannot unsuppress data in setups that you save with Save only Unsuppressed data in the Save As dialog box.

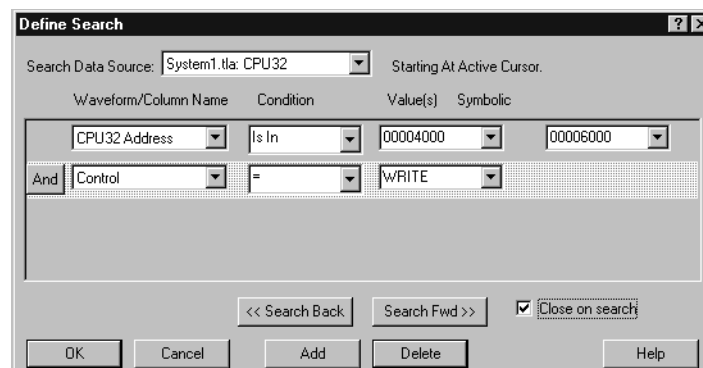


Figure 3–61: Defining search criteria

Locking Windows

Locking windows provides an easy method to compare data from two different windows. Use the Lock Windows dialog box, shown in Figure 3–62, to select how windows are locked together.

To open the Lock Windows dialog box go to the System window and click the button for the data window you want to open. Go to the View menu and then select Lock Windows.

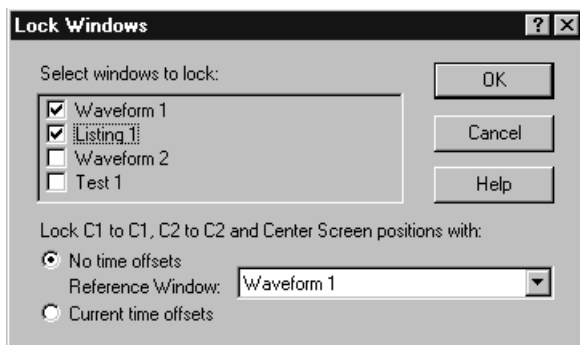


Figure 3–62: Lock Windows dialog box

MagniVu Data

The LA modules have MagniVu data acquisition as a standard feature. MagniVu data acquisition offers 500 picosecond, high-speed timing simultaneous with 200 MHz state on all channels through the same probe; no double probing is required. The record length for MagniVu data is 2000 samples.

You can view MagniVu data in both Listing and Waveform windows. For more information on MagniVu data, refer to *MagniVu Data* beginning on page 3–72.

Comparing Listing Data

When comparing data against reference data, you can highlight data that is equal to or not equal to the reference data.

NOTE. Before you can display compare data, you must define the compare parameters in the Define Compare dialog box in the LA Setup window. Refer to Memory Compare beginning on page 3–5 for information on setting up the compare parameters.

The following steps describe how to display compare data in the Listing window.

1. Open a Listing window and click the Properties tool bar button, as shown.



2. Select the Listing Window property page.
3. Select Show Compare, and select one of the colors for when data does not equal the reference data (Acq!=Ref). See Figure 3–63.
4. If you want to highlight data that does equal the reference data, select Acq=Ref and the appropriate color.

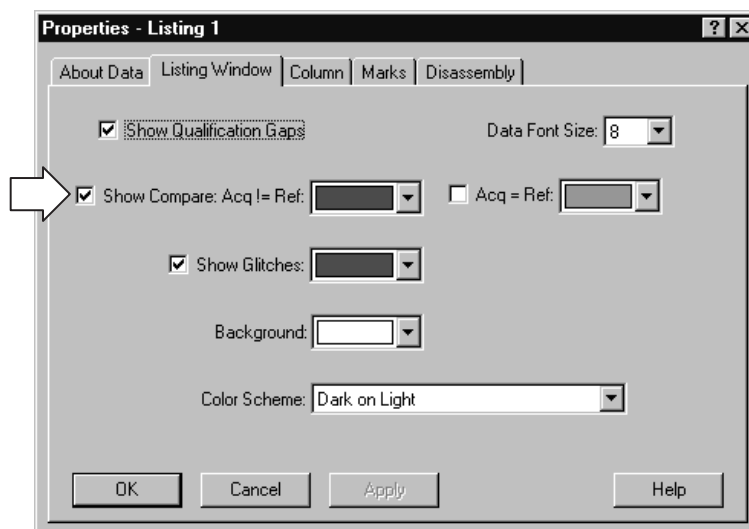


Figure 3–63: Selecting compare data colors in the Listing Window property page

5. Click OK.

The data differences or equalities will be highlighted in colors you specified, similar to Figure 3–64.

NOTE. For more information on comparing data, refer to Guidelines for Memory Compare on page 3–7.

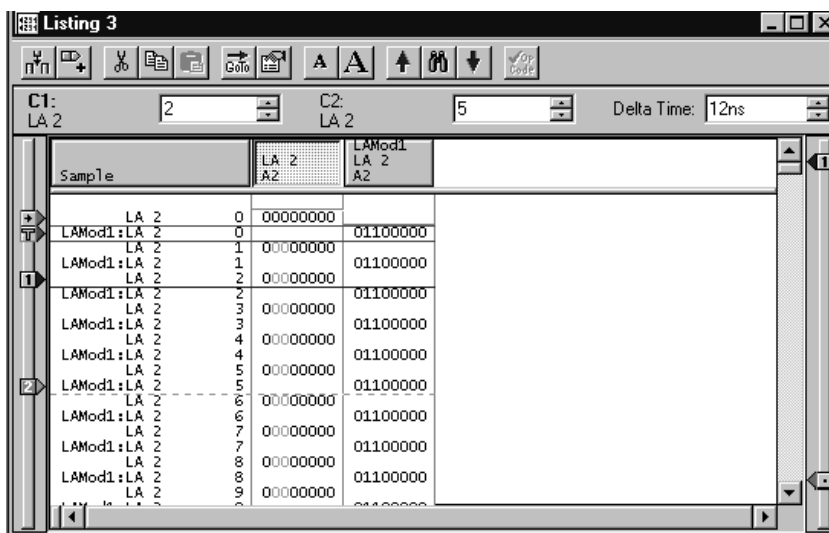
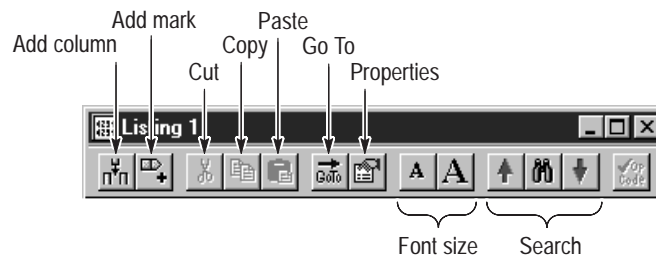


Figure 3–64: Viewing LA compare data in a Listing window

Adjusting the Listing Data View

There are a number of actions you can perform in the Listing window to get the exact view of the data that you want.

Listing Window tool bar The tool bar has shortcut buttons for common operations, as shown below.



Changing the Display Font Size Click the Font Size tool bar buttons. Continue to click the tool bar buttons until the text reaches the desired size. You can also set the font to a specific size in the Listing Window property sheet.

Moving Columns Select the column labels and then drag them to their new location.

Adding a New Column or Data Source Click the tool bar Add Column button to open the Add Column dialog box. Then select the data source and its associated group or channel to add it to the display. If the data source you want is not listed, click Add Source and find and select the source. The data source can be an installed module or a saved module file. See Figure 3-65.

New columns are added after (to the right of) the selected columns or after all columns if none are selected.

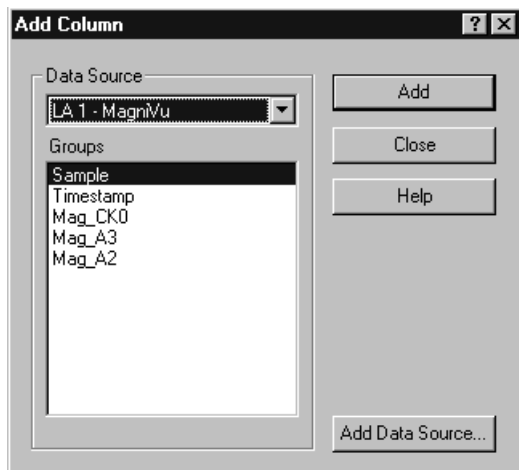


Figure 3–65: Add Column dialog box

Deleting Columns

Select the column labels, then click the Cut tool bar button.

Changing Column Width

Double-click the column label to open the Column Properties page. Enter a new value for the column width. If you have a portable mainframe, you can also change the column width by selecting the column label and use the front panel Scale control to set the width.

Cut, Copy, Paste

You can cut, copy, and paste columns and marks. You can also copy textual data from the listing to the clipboard. From there you can paste it to other areas, such as the Define Search dialog box or the Clause Definition dialog box in the Trigger window.

Changing Radixes

To change a column radix in the Listing window, double-click the column label to open the Column Properties page. Select a new radix. To select the Symbolic radix, you must have loaded a symbol table. See *Symbol Support* beginning on page 2–44 for information about using symbols and symbol table files.

Viewing Qualification Gaps

Qualification gaps indicate that data samples were not stored due to storage qualification or Don't Store trigger actions.

Qualification gaps are indicated with a horizontal gray line above the first data after the gap. Turn qualification gaps on or off from the Listing Window property page.

Viewing Glitches Glitches are indicated by highlighted text of the complete sample for all radices except binary, octal, and hexadecimal. In those radices, only the glitch bits are highlighted. Turn glitches on or off from the Listing Window property page.

***NOTE.** To view glitches in a data window, you must enable Glitch storage in the LA Setup window before acquiring data.*

Naming Columns Rename a column by returning to the LA Setup window and changing the channel group name.

Changing the Disassembly Format For microprocessor support packages, you can change the disassembly format used in the Listing window. Use the Disassembly property page to select the display format of disassembly groups. You must have a support package loaded for this page to be active.

Splitting the Data Area You can split the data area to compare columns that are far away from each other within the display. Drag the split box from the left end of the horizontal scroll bar.

Customizing the Listing Window Data Area

Use property sheets to customize data in the Listing window. The property sheets control aspects of the listing display such as size, color, and in some cases, enabling or disabling whether an element is shown. Click the Properties tool bar button to open the Listing Window property sheet. Then select one of the property sheets to change the data you are interested in.

Exporting Listing Data

Use the Export Data dialog box to export data from the current listing window to a text file or to a binary file. This is a way to print a copy of a complete or partial listing. Figure 3–66 shows the Export Data dialog box.

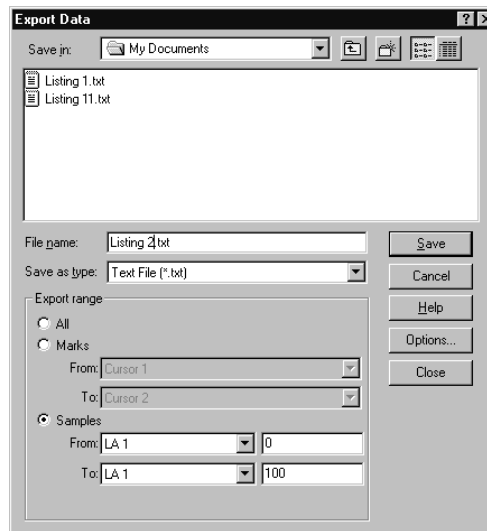


Figure 3–66: Export Data dialog box

You can export the following listing data:

- All listing data from the acquisition
- Listing and DSO voltage measurement from a Listing window
- A range of listing data between two selected marks
- A range of listing data between two samples

Exporting Data to an ASCII File

If you want to export data to a text file, click Options to define the format of the data in the Export Data Options dialog box (see Figure 3–67). The data is saved in a text file with the .txt file name extension.

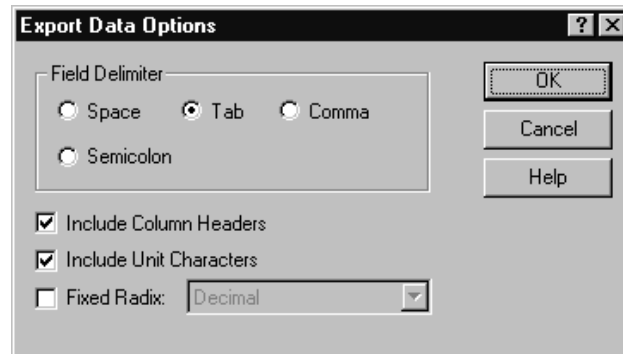


Figure 3–67: Export Data Options dialog box

Use the Export Data Options dialog box to customize the listing data for a text file. You can specify the field delimiter to separate the listing columns. You can also specify that measurement units should be included with the data. If you export the data without unit characters, the time stamp values are in picoseconds and the DSO values are listed in volts.

To export listing data, follow these steps:

1. In the System window, select a Listing window.
2. Select Export Data from the File menu.
3. In the Export Data dialog box, select the folder to which you want to export data. Otherwise, leave the default of My Documents.
4. Click Options to specify any export options for the text data and then click OK.
5. Enter a name for the exported file.
6. Specify the export range.
7. Click Save.

Exporting Data as a Binary File

You can also export the listing data as a binary file with a .tbf (TLA700 Binary Format) file name extension. This option is only available if the data window is from a single data source. You can export any data that appears in a Listing window, including DSO and MagniVu data. This option is useful when you write applications that need to use binary data. It is also faster than exporting an ASCII file and the file size is often smaller.

LA Module Binary Export File Format. The LA module binary data is exported as a stream of bytes with the following characteristics:

- The binary data uses big-endian fields (the most significant bit is the left-most bit).
- Each group column field is zero-padded on the most significant end to the nearest byte.
- Sample numbers and mnemonics groups are not exported.
- Time stamp data is seven bytes wide and represents the number of picoseconds since the start of the acquisition.
- The left-most column in the Listing window display corresponds to the first exported field of a sample.
- The first sample in the Listing window appears at the beginning of the exported file.
- MagniVu data follows the same guidelines as regular listing data.

DSO Module Binary Export File Format. The DSO module binary data (when used in a Listing window) is exported as a stream of bytes with the following characteristics:

- The binary data uses little-endian fields (the most significant bit is the right-most bit).
- Each channel field is a 16-bit value.
- Sample numbers, mnemonics groups, and time stamp values are not exported.
- The left-most column in the Listing window display corresponds to the first exported field of a sample.
- The first sample in the Listing window appears at the beginning of the exported file.
- DSO data values are in twos-compliment format.
- The formula used for converting a DSO channel field into a voltage is:

$$((\text{Vertical range in volts} / 64512) \times \text{channel field}) + \text{vertical offset in volts}$$

The contents of the window will be sent to the printer or to the specified file.

Listing Window Shortcut Keys

You can use the general purpose shortcut keys listed in Table 3–10 to move data and cursors in the Listing window. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- CTRL + Arrow keys move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3–10: Listing window shortcut keys

Desired action	Key combination
Go to next trigger	CTRL + T
Display Go To dialog box	CTRL + G
Move Cursor 1 to the center of the window	CTRL + 1
Move Cursor 2 to the center of the window	CTRL + 2
Add a mark	CTRL + K
Add a column	CTRL + L
Scroll data up 10 samples	Shift + Up arrow
Scroll data down 10 samples	Shift + Down arrow
Move active cursor up one sample	CTRL + Up arrow
Move active cursor down one sample	CTRL + Down arrow
Move active cursor up 10 samples	CTRL + Shift + Up arrow
Move active cursor down 10 samples	CTRL + Shift + Down arrow

Source Window

Use the Source window to display the high-level language (HLL) source code as it is executed by your target system and acquired by the logic analyzer. The logic analyzer links the Source and Listing windows, and provides additional tools to help you view the tools and data. See Figure 3–68 for an example of a Source window.

The data area of the Source window lists the content of the source file including line numbers for each source code statement. The path name of the file displays immediately above the source data.

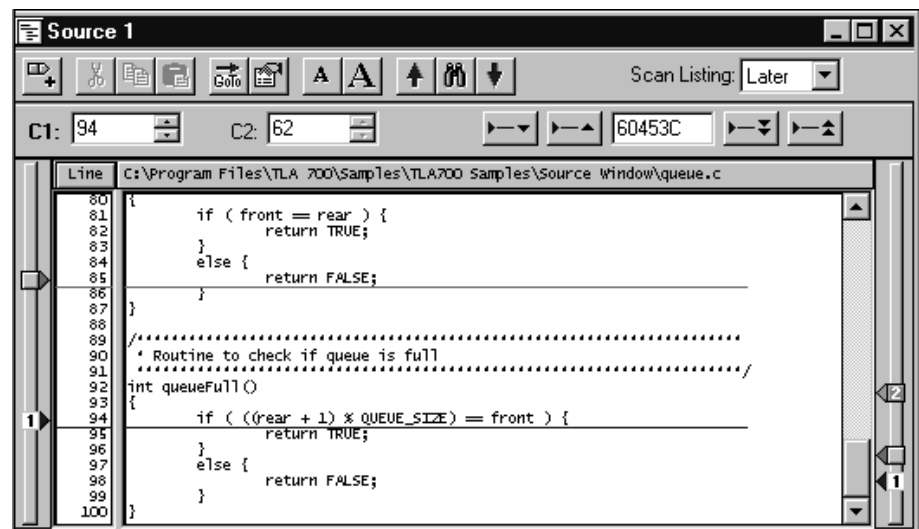


Figure 3–68: Source window

You can use controls to step through data, move between user-defined marks, and scroll through data. These controls directly affect the active cursor in the associated Listing window and indirectly affect the active cursor in the Source window.

Creating a Source Window

Before creating a Source window load a microprocessor support package. You should also set up the Listing window you will use with the Source window.

Create a new Source window with the New Data Window wizard. You can access the New Data Window wizard from the tool bar in the System window. For help on using the New Data Window wizard, refer to the online help.

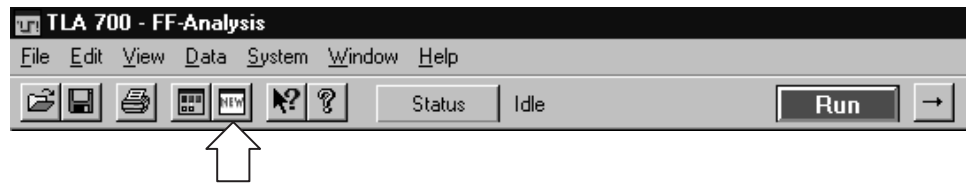


Figure 3–69: Accessing the New Data Window wizard

Reading the Source Window Indicators

Data marks, cursors, and other indicators help you navigate and identify the data. Figure 3–70 and Table 3–11 identify and describe data window marks.

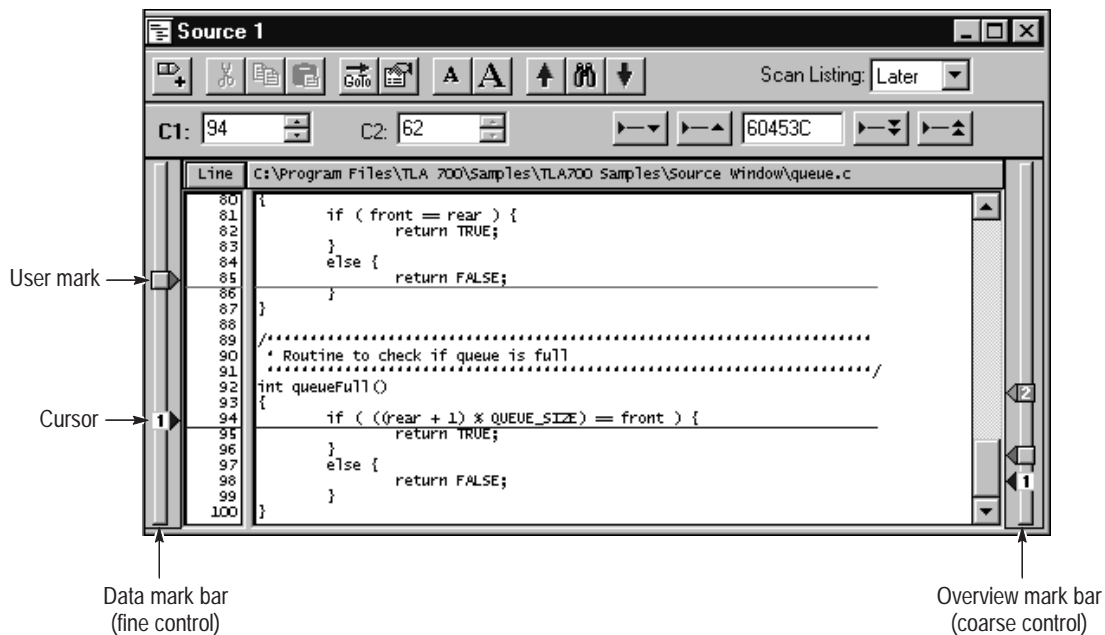


Figure 3–70: Source window cursors and marks

Table 3–11: Source window cursor and mark summary

Mark	Name	Description
1 2	Cursors 1 and 2	Moveable marks used for visual reference and for data measurements.
<input type="checkbox"/>	User mark	User-created marks. Use marks to make specific data more easy to identify and find.

Jumping to Specific Data Locations

You can use the Go To dialog box to jump to a new position by selecting any current mark or waveform. To open the Go To dialog box, open a data window, and click the Go To tool bar button, as shown in Figure 3–71.

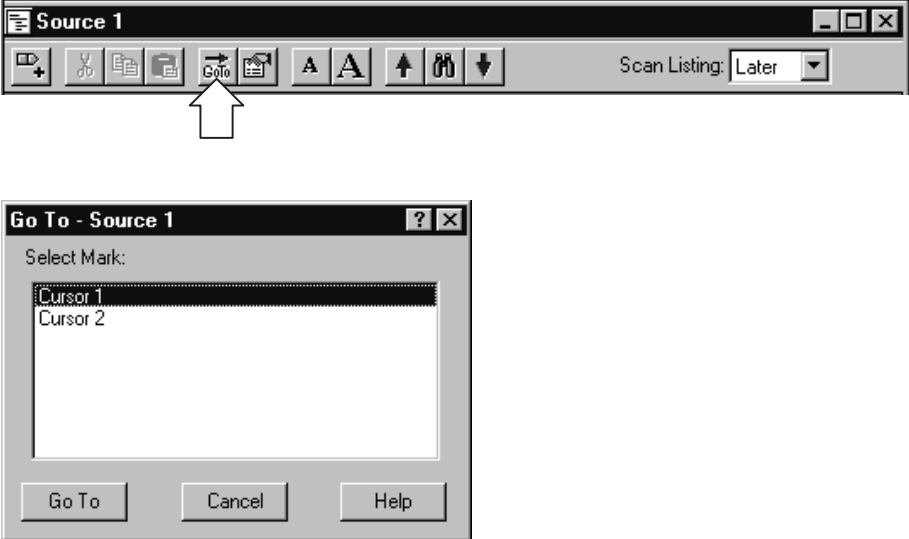


Figure 3–71: Using the Go To dialog box to jump to the cursor location

You can also use the Overview Mark bar to quickly jump to another location. If you do not click on a mark, clicking in the Overview Mark bar scrolls to that location.

Moving the cursor between statements in the Source window does not necessarily move the cursor in the same direction in the Listing window. This can happen, for example, if the statement in the new location was executed both before and after the statement in the old location, such as when the statement is in a loop. The Scan Listing box sets the scan direction in a Listing window when you move the cursor in the Source window.

Moving Through Source Files

There are several ways of moving through the data in source files. You can move through source files from the Source window or from the Listing window. When you move a cursor in one window, the corresponding cursor in the other window also moves.

Use the Step Forward or the Step Backward buttons (see Figure 3–72) to step through source statements in execution order in the Source window. You can also use the Next Mark or the Previous Mark buttons to jump to the next or previous executed source statement that has a user-defined mark.

Use the cursor controls in either window to move the cursors. You can also move the cursors in either window by clicking and dragging the cursor handles or by adjusting the cursor spin box controls.

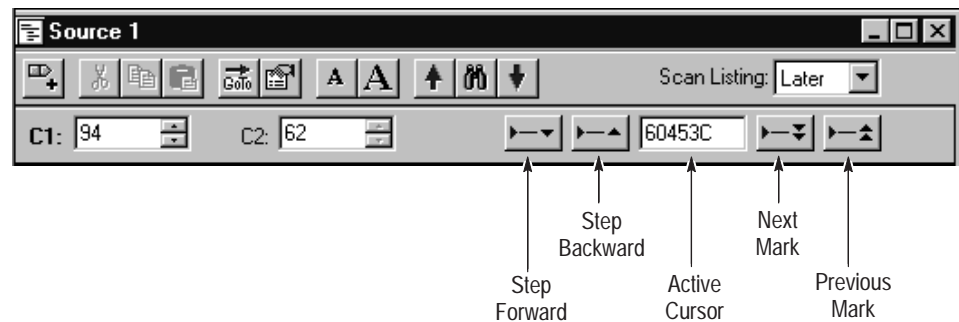


Figure 3–72: Source window controls

Source-Relative Cursor Positioning

Source-relative cursor positioning refers to updating the Listing window cursor positioning as a result of changing the position of the active cursor in the Source window.

When you move the Source window cursor to a new statement, the Source window determines the address range of the source statement based on information from the loaded symbol file. The Source window uses the setting of the Scan Listing mode to determine the search direction in the Listing window. The Listing window searches the acquisition data for a matching address. When the matching address is found, the active cursor in the Listing window is moved to the matching sample.

If the Source window cursor is moved to a non-executable statement, such as a comment, the address of the next executable statement is used.

Listing-Relative Cursor Positioning

Listing-relative cursor positioning refers to updating the Source window cursor position of the active cursor in the Listing window.

When you move the Listing window cursor to a new sample, the active Source window cursor attempts to move to a corresponding source statement in the Source window. The Source window uses information from the loaded symbol file to convert the address of the Listing cursor position to a source file name and statement (line number) location. The Source window then updates the active Source window cursor position and displays the corresponding source statement.

Step Forward and Step Backward Buttons

Use the Step Forward and Step Backward buttons to trace the execution order of source statements. Click the Step Forward button to move to the next executed source statement. Click the Step Backward button to move to the previous executed source statement.

When you click the Step Forward or Step Backward buttons, the Source window tells the Listing window to search forward or backward beginning at the active Listing cursor for the next or previous executed source statement. When a match is found, the Listing window positions the active Listing cursor to the matching sample. The Source window converts the address to a file name and line number, and then updates the active Source cursor position to the corresponding source statement. The statement may be located in a source file that is different than the original displayed file. In this case, the new file is displayed and the cursor is placed on the proper statement.

A single line in the Source window may consist of more than one statement, for example:

```
for ( i=0; i < NUM_STATES; i++)
```

The next executed statement in the Listing window may appear on the same line in the Source window as the current statement. However, the next executed statement may also appear on a different line (before or after the current statement), or in a different file. Click the Step Forward and Step Backward buttons to move the cursor between statements in execution order.

The ability of the Source window to discriminate between multiple statements on the same line depends on the amount of information provided by the code generation tools. If there is enough information to identify multiple statements per line, the Source window cursors will include character highlighting to identify individual statements on a line.

Next Mark and Previous Mark Buttons

Use the Next Mark and Previous Mark buttons to move the active cursor in the Source window to the next or previous executed user-defined mark position (if any marks have been defined). Next and previous refer to the execution sequence and not to the position of the mark in the window.

The Next Mark and Previous Mark buttons operate similar to the Step Forward and Step Backward buttons. However, rather than stepping through every executed statement, you can define marks in the Source window as breakpoints and then step between marks in execution order to move through the source code.

When you click the Next Mark or Previous Mark buttons, the Source window tells the Listing window to search for addresses corresponding to the marked source statements. When a corresponding sample is found, the Listing window positions its active cursor to the matching sample. The Source window converts the address to a file name and line number. It then updates the active Source cursor position and displays the corresponding source statement.

If the code generation tools provide column information for symbol files, you can mark individual statements of multiple-statement lines in the source code. You can then use the Next Mark and Previous Mark buttons to step between the marks and highlight the individual statements.

The Next Mark and Previous Mark buttons are not active if there are no marks defined in the Source window.

Active Cursor Readout

The active cursor readout displays the address of the source statement at the active cursor. The address shown is the low address bound. The radix of the address is always hexadecimal. If you position the cursor on a non-executable statement, such as a comment or white space, the address of the next executable statement is displayed.

Use the active cursor readout to jump to a new location in the source file. Enter an address in this field and the active cursor moves to the corresponding statement. If you enter an address that does not correspond directly to the address of a source statement, the next statement will be used and the address is adjusted.

You can copy and paste the readout value into other locations such as in the event portion of the Clause Definition dialog in the LA Trigger window.

Uncorrelated State

There are situations when you move the cursor in the Listing window to a location where there is no corresponding source statement. The cursor in the Source window remains at the current location and changes the color of the Source window to signify that an uncorrelated state exists between the Source and Listing windows. When this happens, you can click the Step Forward or the Step Backward buttons to search for an executable source line in the Listing window; this correlates the active cursors in both windows.

Clicking the buttons forces the Listing window to search for a data sample that corresponds to the next or previous line of executed source code. The line of executed code may be in a different source file. If this happens, the Source window displays the required file or prompts you for a path name. The ability to locate source files depends on the Search Path List and Suffix List defined in the Source Files property page.

Searching for Source Data

Use the Define Search dialog box to search for specific text patterns. You can search the current source file or search all of the source files identified by the loaded symbol file.

Click on the search icon to open the dialog box and then fill out the search conditions (see Figure 3–73). The active cursor marks the first occurrence of the data.

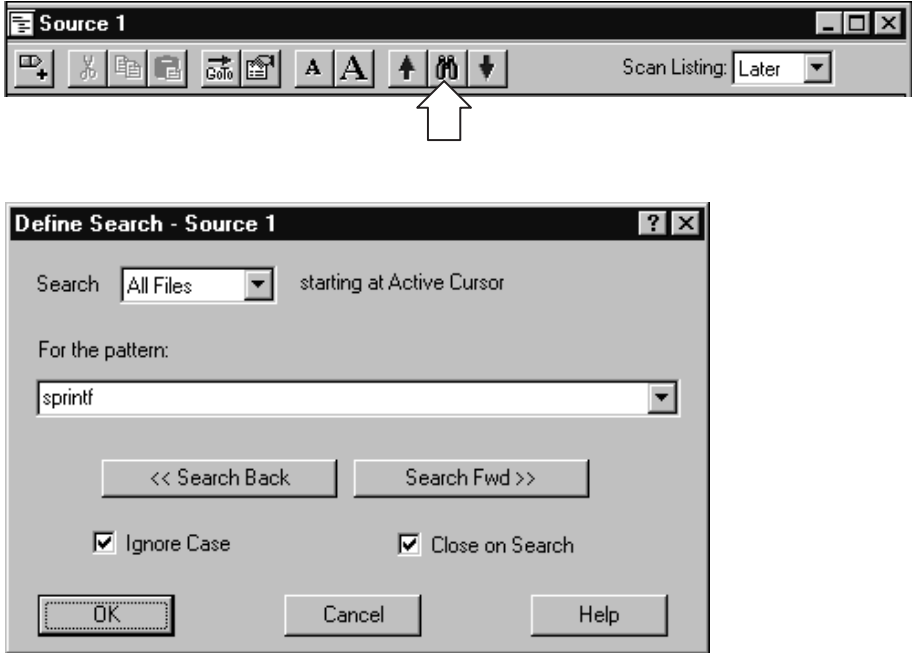


Figure 3–73: Defining source search criteria

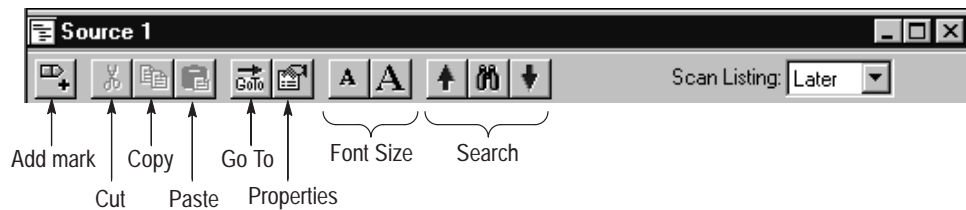
You can search for any text pattern including leading and embedded white space; trailing white space is ignored.

When searching for data in multiple files, the search operation follows the order of files listed in the Source Window property page in the Displayed Source File list. When you search for data in all files and one or more of the files cannot be found, the Source File Locator dialog box displays, asking you to specify the location of the file.

If the search is not completed in a set amount of time, the Search Progress dialog box shows the status of the search. You can let the search continue, or you can click Abort to stop the search.

Adjusting the Source Data View

There are a number of actions you can perform in the Source window to get the exact view of the data that you want. You can access most of the shortcuts from the Source window tool bar.



Changing the Display Font Size

Click the Font Size tool bar buttons, shown in the previous figure. You can continue to click the tool bar buttons until the text reaches the desired size. You can also set the font to a specific size in the Source window property sheet.

Cut, Copy, Paste

You can cut, copy, and paste columns and marks. You can also copy text data to the clipboard. From there you can paste it to other areas, such as the Define Search dialog box or the Clause Definition dialog box in the Trigger window.

Turning Line Numbers On or Off

Turn source line numbers on or off by clicking Line Number Column in the View menu.

Customizing the Source Window Data Area

Use property sheets to customize data in the Source window. The property sheets control aspects of the source display such as source files, text size, colors, tab spacing, and source file locations. Click the Properties tool bar button to open the Source window property sheet. You can also click the label above the data area to open the property sheet. Then select one of the property sheets to change the data you are interested in.

Locating Source Files

You can define the location of source files with the Source Files property page (see Figure 3–74). Use the property page to list the locations of source files as well as possible file suffixes that can be attached to the file names (used for compilers that do not include the file suffixes). A similar property page (System Source Files property page) is used as a default list of locations of source files and suffixes. The logic analyzer uses this list every time you create a new source window.

The Source window uses the file path and file suffix in combination to locate the correct source file. It searches for the file name in each directory indicated by the file path list in the order specified. If a file name does not have a suffix, then suffixes from the suffix list are tried until a match is found or all file path and suffix combinations are exhausted.

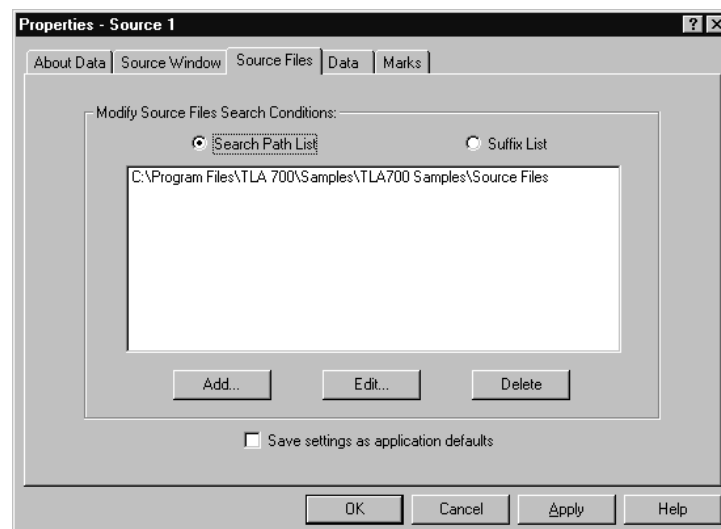


Figure 3–74: Source Files property page

When specifying the search path, you can use an asterisk (*) as the final component of a search path directory. For example, if you specify the following path, C:\MySources*, the MySources directory and all directories (one level deep) within MySources will be searched. However, you cannot use the asterisk as a general-purpose wild card character. For example, the use of an asterisk in C:\MySources** or C:\MySources\abc* is invalid.

You must specify the complete absolute (not relative) path name for the file in the Search Path List. Otherwise, the Source window will not locate the source file. Make sure that the source file you are looking for has a unique file name. When searching for source files it is possible to load the wrong file if there is another file with the same name in the directories specified by the search path. The Source window always loads the first file that matches the search criteria.

Because some compilers do not include a source file suffix, you may also need to specify the correct file suffixes in the file suffix list (examples of correct file suffixes are: .c, .cpp, and .s). The Source window will always load the first file that matches the criteria in the file suffix list.

The logic analyzer searches for files using both lists from top to bottom. Therefore, you should place the most likely search path or file suffix at the beginning of the lists.

The search path lists and the suffix lists in the Source Files property page are valid only for the current Source window. If you want to save the settings as defaults, click Save settings as application defaults near the bottom of the window (see Figure 3-74 on page 3-103). The settings will be saved to System Source Files property page and will be used each time you create a new Source window.

Source Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–12 to move data and cursors in the Source window. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- CTRL + Arrow keys move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3–12: Source window shortcut keys

Desired action	Key combination
Display Go To dialog box	CTRL + G
Move Cursor 1 to the center of the window	CTRL + 1
Move Cursor 2 to the center of the window	CTRL + 2
Add a mark	CTRL + K
Scroll data up 10 lines	Shift + Up arrow
Scroll data down 10 lines	Shift + Down arrow
Move active cursor up one line	CTRL + Up arrow
Move active cursor down one line	CTRL + Down arrow
Move active cursor up 10 lines	CTRL + Shift + Up arrow
Move active cursor down 10 lines	CTRL + Shift + Down arrow

Histogram Window

Use the Histogram window to set up, capture, and display performance analysis data from an LA module channel group, counter, or timer. You can use the Histogram window to determine the level of activity within various functions or subroutines, analyze how memory is used, or determine the relative execution time of subroutines or program modules.

Histogram data is presented as a list of ranges and corresponding histogram bars showing the distribution of the ranges. See Figure 3–75 for an example.

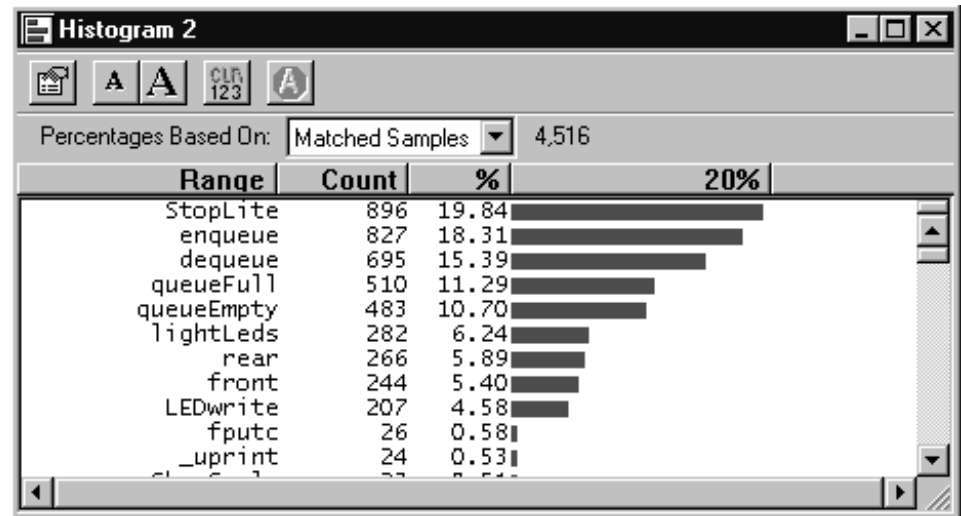


Figure 3–75: Histogram window

The histogram data is based on all acquisition data (All Samples) or on the data within a defined set of ranges (Matched Samples).

Measuring Histogram Data

There are two basic ways of using the Histogram window to analyze data. One is to provide a graphic overview of the address activity of software execution. The other is to use counters or timers to measure specific events.

If you want to use counters or timers to measure events, you must set up the counters or timers in the Trigger window. You can then select the data source in the New Data Window wizard when you create a Histogram window. You can also select the data source for an existing Histogram window from the Data Source property page as shown in Figure 3–76.

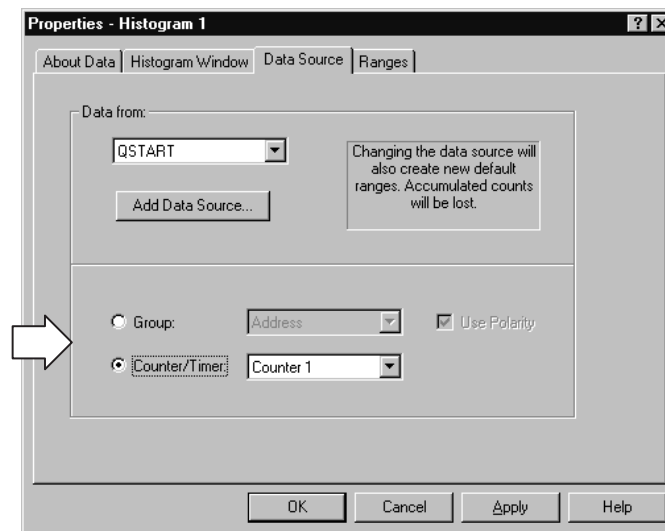


Figure 3–76: Selecting the data source for the Histogram window

Viewing Address Activity for Channel Groups (Range Overview)

To provide an overview of the address activity of a software routine, you define a set of ranges (either numeric, logarithmic, or symbolic). You can set up the Trigger window to look for data within the defined ranges. The data is processed and displayed in the Histogram window for the current acquisition. If you set up the logic analyzer to repetitively acquire data, the sampling errors will decrease over time as you acquire more data. The resultant data provides a stable display in the Histogram window where you can view the overall activity of the software.

You can use this method of analyzing data to determine which sections of code are being accessed or not accessed. You can also determine the time spent in a routine relative to other areas of code. Figure 3–75 is an example of viewing address activity in a software application using symbolic ranges.

Measuring Counter or Timer Events (Single Event)

To measure an event, you define a starting point, a target event, a counter or a timer, and a stopping point in the LA Trigger window. Use the Data Source property page to select the counter or timer as the data source for your analysis. When you acquire data, the Histogram window displays the minimum, maximum, and average value of the counter or timer data as shown in Figure 3–77.

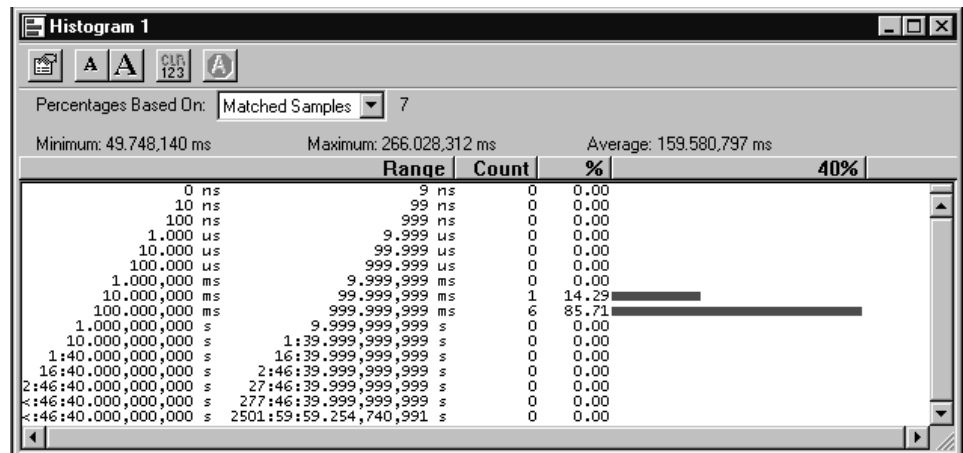
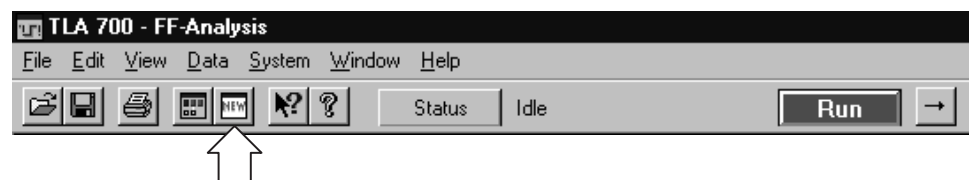


Figure 3–77: Measuring events with the Histogram window

Creating a Histogram Window

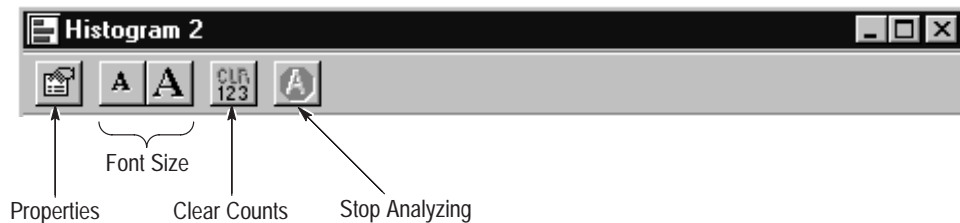
Before creating the Histogram window, define the channel setups and clocking in the Setup window. You should also define your trigger program in the Trigger window. If you want to measure an event, you should define the trigger events and set up the appropriate counter and timer actions. If you want to use symbols, you should make sure that you load the symbol file.

Create a new Histogram window with the New Data Window wizard. You can access the New Data Window wizard from the tool bar in the System window. For help on using the New Data Window wizard, refer to the online help.



Adjusting the Histogram Data View

There are a number of actions you can perform in the Histogram window to get the exact view of the data that you want. Use the buttons in the tool bar to access short cuts to adjust the data view.



Changing the Display Font Size

Click the Font Size tool bar buttons, shown in the previous figure. Continue to click the tool bar buttons until the text reaches the desired size. You can also set the font to a specific size in the Histogram Window property sheet.

Clearing Histogram Counts

Click the Clear Counts tool bar button to reset all ranges and percentages to zero.

Stopping Analysis

Click the Stop Analyzing tool bar button to stop analyzing the current acquisition. This button is inactive when there is no current acquisition in process.

Sizing Columns

Select the column label separator and drag it to change the width of a column.

Sorting Data within Columns

Sort ranges, counts, and percentages by clicking on the column labels. Click the column label to toggle the sort between increasing and decreasing values.

Changing Histogram Magnification

Select Scale from the View menu. Select a new magnification value from the list and click OK. You can also click on the percentage column label and select a magnification value.

Defining Histogram Ranges

Ranges displayed in the Histogram window are based on the values you select in the Ranges property page. You can define ranges as follows:

- Linear generation. The ranges are divided linearly between two bounds.
- Log generation. The ranges are divided logarithmically between two bounds.
- Symbols. The ranges are defined by the values in a loaded symbol file. You can use the same loaded symbol table as in other windows.

Splitting the Data Area You can split the data area to compare ranges that are far away from each other within the display. Drag the split box from the top of the horizontal scroll bar.

Customizing the Histogram Window Data Area

Use property sheets to customize data in the Histogram window. The property sheets control aspects of the Histogram display such as ranges, bounds, font size, color, and data source information. Click the Properties tool bar button to open the property sheets. Then select one of the specific property sheets you are interested in.

Here are some guidelines for using and customizing the Histogram window.

- Data is accumulated until you explicitly clear the data.
- There is no limit to the number of symbolic ranges for histogram data.
- You can analyze live LA data or saved LA data (reference data).
- You can use up to 32 bits of data in a address group.
- You can enable or disable channel group polarity.
- You can change colors for the foreground, background, and histogram bars as needed.
- You can change the data font size as necessary to view the data.

Exporting Histogram Data

Use the Export Histogram dialog box to export data from the current Histogram window to a text file. This is a way to print a copy of the histogram data. Figure 3–78 shows the Export Histogram dialog box.

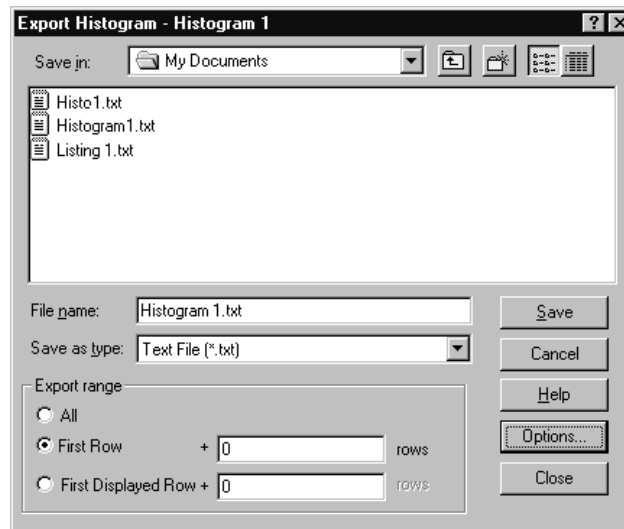


Figure 3–78: Export Histogram dialog box

Click Options to define the format of the data in the Export Histogram Options dialog. The data is saved in a text file with the .txt file name extension.

Use the Export Data Options dialog to customize the data for a text file. You can specify the field delimiter to separate the columns. To export the bounds as a text string, select Label “00–FF.” To export the bounds as two delimited numbers, select Numbers.

To export Histogram data, follow these steps:

1. In the System window, select a Histogram window.
2. Select Export Histogram from the File menu.
3. In the Export Histogram dialog box, select the folder to which you want to export data. Otherwise, leave the default of My Documents.
4. Click Options to specify any export options for the text data and then click OK.
5. Enter a name for the exported file.

6. Specify the export range.

7. Click Save.

Figure 3–79 shows an example of an exported histogram file.

Range	Count	%
"0-0"	5	6.41
"1-1"	5	6.41
"2-2"	5	6.41
"3-3"	5	6.41
"4-4"	5	6.41
"5-5"	5	6.41
"6-6"	5	6.41
"7-7"	5	6.41
"8-8"	5	6.41
"9-9"	5	6.41
"A-A"	4	5.13
"B-B"	4	5.13
"C-C"	5	6.41
"D-D"	5	6.41
"E-E"	5	6.41
"F-F"	5	6.41

Figure 3–79: ASCII histogram data file

Histogram Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–13 to move data and cursors in the Histogram window. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- The Shift key increases movement by a factor of 10.

Table 3–13: Histogram window shortcut keys

Desired action	Key combination
Scroll data up 10 ranges	Shift + Up arrow
Scroll data down 10 ranges	Shift + Down arrow



Appendices

Appendix A: Specifications

This chapter lists the specifications for the Tektronix Logic Analyzer family and the associated modules.

Characteristic Tables

All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Tektronix Logic Analyzer Family Performance Verification and Adjustment Technical Reference Manual*.

For mainframes and modules, the performance limits in this specification are valid with these conditions:

- The logic analyzer must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The logic analyzer must have had a warm-up period of at least 30 minutes.

For modules, the performance limits in this specification are valid with these conditions:

- The modules must be installed in a Logic Analyzer Mainframe.
- The module must have been calibrated/adjusted at an ambient temperature between +20°C and +30°C.
- The DSO module must have had its signal-path-compensation routine (self calibration or self cal) last executed after at least a 30 minute warm-up period.
- After the warm-up period, the DSO module must have had its signal-path-compensation routine last executed at an ambient temperature within $\pm 5^{\circ}\text{C}$ of the current ambient temperature.

Atmospheric Characteristics for the Tektronix Logic Analyzer Family

Table A–1 lists the Atmospheric characteristics of all components in the Tektronix Logic Analyzer family.

Table A–1: Atmospheric characteristics

Characteristic	Description
Temperature: Operating and nonoperating	<p>Operating (no media in floppy disk drive): +5°C to +50°C, 15°C/hr maximum gradient, non-condensing (derated 1°C per 1000 ft above 5000 foot altitude)</p> <p>Nonoperating (no media in floppy disk drive or CD ROM drive): –20°C to +60°C, 15°C/hr maximum gradient, non-condensing.</p>
Relative Humidity: Operating and nonoperating	<p>Operating (no media in floppy disk drive or CD ROM drive): 20% to 80% relative humidity, non-condensing. Maximum wet bulb temperature: +29°C (derates relative humidity to approximately 22% at +50°C).</p> <p>Nonoperating (no media in floppy disk drive or CD ROM drive): 8% to 80% relative humidity, non-condensing. Maximum wet bulb temperature: +29°C (derates relative humidity to approximately 22% at +50°C).</p>
Altitude: Operating and nonoperating	<p>Operating: To 10,000 ft (3040 m), (derated 1°C per 1000 ft (305 m) above 5000 ft (1524 m) altitude)</p> <p>Nonoperating: 40,000 ft (12190 m).</p>

Certifications and Compliances

Table A–2 lists the certifications and compliances of the Tektronix Logic Analyzer family. The certifications and compliances apply to all components of the Tektronix Logic Analyzer family unless noted otherwise.

Table A–2: Certifications and compliances

Characteristic	Description																
EC Declaration of Conformity – EMC	<p>Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:</p> <table> <tr> <td>EN 61326–1</td> <td>EMC requirements for Class A electrical equipment for measurement, control and laboratory use.</td> </tr> <tr> <td>IEC 1000–4–2</td> <td>Electrostatic Discharge Immunity (Performance Criterion B)</td> </tr> <tr> <td>IEC 1000–4–3</td> <td>RF Electromagnetic Field Immunity (Performance Criterion A)</td> </tr> <tr> <td>IEC 1000–4–4</td> <td>Electrical Fast Transient / Burst Immunity (Performance Criterion B)</td> </tr> <tr> <td>IEC 1000–4–5</td> <td>Power Line Surge Immunity (Performance Criterion B)</td> </tr> <tr> <td>IEC 1000–4–6</td> <td>Conducted RF Immunity (Performance Criterion A)</td> </tr> <tr> <td>IEC 1000–4–11</td> <td>Power Line Dips and Interruptions Immunity (Performance Criterion B)</td> </tr> <tr> <td>EN 61000–3–2</td> <td>AC Power Line Harmonic Emissions</td> </tr> </table>	EN 61326–1	EMC requirements for Class A electrical equipment for measurement, control and laboratory use.	IEC 1000–4–2	Electrostatic Discharge Immunity (Performance Criterion B)	IEC 1000–4–3	RF Electromagnetic Field Immunity (Performance Criterion A)	IEC 1000–4–4	Electrical Fast Transient / Burst Immunity (Performance Criterion B)	IEC 1000–4–5	Power Line Surge Immunity (Performance Criterion B)	IEC 1000–4–6	Conducted RF Immunity (Performance Criterion A)	IEC 1000–4–11	Power Line Dips and Interruptions Immunity (Performance Criterion B)	EN 61000–3–2	AC Power Line Harmonic Emissions
EN 61326–1	EMC requirements for Class A electrical equipment for measurement, control and laboratory use.																
IEC 1000–4–2	Electrostatic Discharge Immunity (Performance Criterion B)																
IEC 1000–4–3	RF Electromagnetic Field Immunity (Performance Criterion A)																
IEC 1000–4–4	Electrical Fast Transient / Burst Immunity (Performance Criterion B)																
IEC 1000–4–5	Power Line Surge Immunity (Performance Criterion B)																
IEC 1000–4–6	Conducted RF Immunity (Performance Criterion A)																
IEC 1000–4–11	Power Line Dips and Interruptions Immunity (Performance Criterion B)																
EN 61000–3–2	AC Power Line Harmonic Emissions																
EC Declaration of Conformity – Low Voltage	<p>Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities:</p> <p>Low Voltage Directive 73/23/EEC</p> <table> <tr> <td>EN 61010-1:/A2 1995</td> <td>Safety requirements for electrical equipment for measurement, control, and laboratory use</td> </tr> </table>	EN 61010-1:/A2 1995	Safety requirements for electrical equipment for measurement, control, and laboratory use														
EN 61010-1:/A2 1995	Safety requirements for electrical equipment for measurement, control, and laboratory use																
Approvals	<p>UL3111–1 – Standard for electrical measuring and test equipment</p> <p>CAN/CSA C22.2 No. 1010.1 – Safety requirements for electrical equipment for measurement, control and laboratory use</p>																
Installation Category Descriptions	<p>Terminals on this product may have different installation category designations. The installation categories are:</p> <table> <tr> <td>CAT III</td> <td>Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location.</td> </tr> <tr> <td>CAT II</td> <td>Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected.</td> </tr> <tr> <td>CAT I</td> <td>Secondary (signal level) or battery operated circuits of electronic equipment.</td> </tr> </table>	CAT III	Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location.	CAT II	Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected.	CAT I	Secondary (signal level) or battery operated circuits of electronic equipment.										
CAT III	Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location.																
CAT II	Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected.																
CAT I	Secondary (signal level) or battery operated circuits of electronic equipment.																

Table A-2: Certifications and compliances (Cont.)

Characteristic	Description
Conditions of Approval (TLA700 series only)	Safety Certifications/Compliances are made for the following conditions: Temperature (operation): +5°C to +40°C Altitude (maximum operation): 2000 meters
IEC Characteristics	Equipment type: Test and Measuring Installation Category II Pollution Degree 2 Safety Class I

TLA600 Series Logic Analyzer Specifications

Tables A–3 through A–17 list the specifications for the TLA600 series logic analyzer.

Table A–3: TLA600 input parameters with probes

Characteristic	Description
✓ Threshold Accuracy	± 100 mV
Threshold range and step size	Setable from +5 V to –2 V in 50 mV steps
Threshold channel selection	16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).
✓ Channel-to-channel skew	≤ 1.6 ns maximum
Channel-to-channel skew (Typical)	≤ 1.0 ns
Sample uncertainty	
Asynchronous:	Sample period
Synchronous:	500 ps
Probe input resistance (Typical)	20 k Ω
Probe input capacitance: P6417, P6434 (Typical)	2 pF
Probe input capacitance: P6418 (Typical)	1.4 pF data channels 2 pF CLK/Qual channels
Minimum slew rate (Typical)	0.2 V/ns
Maximum operating signal	6.5 V _{p-p} –3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum
Probe overdrive: P6417, P6418 P6434	± 250 mV or $\pm 25\%$ of signal swing minimum required beyond threshold, whichever is greater ± 300 mV or $\pm 25\%$ of signal swing minimum required beyond threshold, whichever is greater ± 4 V maximum beyond threshold
Maximum nondestructive input signal to probe	± 15 V
Minimum input pulse width signal (single channel) (Typical)	2 ns
Delay time from probe tip to input probe connector (Typical)	7.33 ns

Table A–4: TLA600 backplane

Characteristic	Description
System Trigger and External Signal Input Latencies ¹ (<i>Typical</i>)	
External System Trigger Input to LA Probe Tip ²	–266 ns
External Signal Input to LA Probe Tip via Signal 3, 4 ³	–212 ns + Clk
External Signal Input to LA Probe Tip via Signal 1, 2 ^{3, 4}	–208 ns + Clk
System Trigger and External Signal Output Latencies (<i>Typical</i>)	
LA Probe Tip to External System Trigger Out ⁵	376 ns + SMPL
LA Probe Tip to External Signal Out via Signal 3, 4 ⁵	
OR function	366 ns + SMPL
AND function	379 ns + SMPL
LA Probe Tip to External Signal Out via Signal 1, 2 ^{4, 5}	
normal function	364 ns + SMPL
inverted logic on backplane	364 ns + SMPL

- ¹ All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.
- ² In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.
- ³ “Clk” represents the time to the next master clock at the destination logic analyzer. In the asynchronous (or internal) clock mode, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. In the synchronous (or external) clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.
- ⁴ Signals 1 and 2 (ECLTRG0, 1) are limited to a “broadcast” mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.
- ⁵ SMPL represents the time from the event at the probe tip inputs to the next valid data sample. In the Normal Internal clock mode, this represents the delta time to the next sample clock. In the MagniVu Internal clock mode, this represents 500 ps or less. In the External clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

Table A-5: TLA600 external signal interface

Characteristic	Description
System Trigger Input	TTL compatible input via rear panel mounted BNC connectors
Input Levels V_{IH} V_{IL}	TTL compatible input $\geq 2.0\text{ V}$ $\leq 0.8\text{ V}$
Input Mode	Falling edge sensitive, latched (active low)
Minimum Pulse Width	12 ns
Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods
Maximum Input Voltage	0 to +5 V peak
External Signal Input	TTL compatible input via rear panel mounted BNC connectors
Input Destination	Signal 1, 2, 3, 4
Input Levels V_{IH} V_{IL}	TTL compatible input $\geq 2.0\text{ V}$ $\leq 0.8\text{ V}$
Input Mode	Active (true) low, level sensitive
Input Bandwidth ¹ Signal 1, 2 Signal 3, 4	50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Accepts signals during valid acquisition periods via real-time gating
Maximum Input Voltage	0 to +5 V peak
System Trigger Output	TTL compatible output via rear panel mounted BNC connectors
Source Mode	Active (true) low, falling edge latched
Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output $\geq 4\text{ V}$ into open circuit $\geq 2\text{ V}$ into 50 Ω to ground $\leq 0.7\text{ V}$ sinking 10 mA
Output Protection	Short-circuit protected (to ground)
External Signal Output	TTL compatible outputs via rear panel mounted BNC connectors
Source Selection	Signal 1, 2, 3, 4, or 10 MHz clock
Output Modes Level Sensitive	User definable Active (true) low or active (true) high
Output Levels V_{OH} V_{OL}	50 Ohm back terminated TTL output $\geq 4\text{ V}$ into open circuit $\geq 2\text{ V}$ into 50 Ω to ground $\leq 0.7\text{ V}$ sinking 10 mA

Table A-5: TLA600 external signal interface (Cont.)

Characteristic	Description
Output Bandwidth ² Signal 1, 2 Signal 3, 4	50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously
Output Protection	Short-circuit protected (to ground)

¹ The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

² The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

Table A-6: TLA600 channel width and depth

Characteristic	Description	
Number of channels	Product	Channels
	TLA601, TLA611, TLA621	32 data and 2 clock
	TLA602, TLA612, TLA622	64 data and 4 clock
	TLA603, TLA613, TLA623	96 data, 4 clock, and 2 qualifier
Acquisition memory depth	Product	Memory depth
	TLA601, TLA602, TLA603, TLA604	64 K or 256 K samples ¹
	TLA611, TLA612, TLA613, TLA614	64 K or 256 K samples ¹
	TLA621, TLA622, TLA623, TLA624	1 M samples

¹ PowerFlex options

Table A-7: TLA600 clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period ¹	4 ns to 50 ms in a 1–2–5 sequence 2 ns in 2x Clocking mode	
✓ Minimum recognizable word ² (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417 or a P6418 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
Synchronous clocking		
Number of clock channels ³	Product	Clock channels
	TLA601, TLA611, TLA621	2
	TLA602, TLA612, TLA622	4
	TLA603, TLA613, TLA623 TLA604, TLA614, TLA624	4 4
Number of qualifier channels ⁵	Product	Qualifier channels
	TLA601, TLA611, TLA621	0
	TLA602, TLA612, TLA622	0
	TLA603, TLA613, TLA623 TLA604, TLA614, TLA624	2 4
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.8 ns Maximum hold time = User interface hold time + 0.2 ns Examples: for a P6417 or a P6418 probe and user interface setup and hold of 2.0/0.0 typical: Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns	
Setup and hold window size (data and qualifiers) (Typical)	Channel-to-channel skew (<i>typical</i>) + (2 x sample uncertainty) Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns	
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.5 ns (Ts) to –7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.	
✓ Maximum synchronous clock rate ⁴	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz (10 ns minimum between active clock edges)	
Demux clocking		
TLA603, TLA613, TLA623 TLA604, TLA614, TLA624	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)	

Table A-7: TLA600 clocking (Cont.)

Characteristic	Description
TLA601, TLA611, TLA621 TLA602, TLA612, TLA622	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA602, TLA612, TLA622 A0(7:0) to D0(7:0) TLA602, TLA612, TLA622
Time between DeMux clock edges ⁴ (Typical)	5 ns minimum between Demux clock edges in full-speed mode 10 ns minimum between Demux clock edges in half-speed mode
Time between DeMux store clock edges ⁴ (Typical)	10 ns minimum between Demux master clock edges in full-speed mode 20 ns minimum between Demux master clock edges in half-speed mode
Data Rate ⁴ (Typical)	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.
Clocking state machine	
Pipeline delays	Each channel group can be programmed with a pipeline delay of 0 through 3 active clock edges.

- 1 It is possible to use storage control and only store data when it has changed (transitional storage).
- 2 Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.
- 3 Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.
- 4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.
- 5 All qualifier channels are stored. For custom clocking there are an additional 4 qualifier channels on C2 3:0 regardless of channel width.

Table A-8: TLA600 trigger system

Characteristic	Description										
Triggering Resources											
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: <table border="0" style="width: 100%;"> <tr> <td>16 word recognizers</td> <td>0 range recognizers</td> </tr> <tr> <td>13 word recognizers</td> <td>1 range recognizer</td> </tr> <tr> <td>10 word recognizers</td> <td>2 range recognizers</td> </tr> <tr> <td>7 word recognizers</td> <td>3 range recognizers</td> </tr> <tr> <td>4 word recognizers</td> <td>4 range recognizers</td> </tr> </table>	16 word recognizers	0 range recognizers	13 word recognizers	1 range recognizer	10 word recognizers	2 range recognizers	7 word recognizers	3 range recognizers	4 word recognizers	4 range recognizers
16 word recognizers	0 range recognizers										
13 word recognizers	1 range recognizer										
10 word recognizers	2 range recognizers										
7 word recognizers	3 range recognizers										
4 word recognizers	4 range recognizers										
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted.										
Glitch detector ^{1,2}	Each channel group can be enabled to detect a glitch										

Table A-8: TLA600 trigger system (Cont.)

Characteristic	Description
Minimum detectable glitch pulse width (Typical)	2.0 ns (single channel with P6417, P6418, or a P6434 probe)
Setup and hold violation detector ^{1,3}	Each channel group can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector ¹	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample. This mode can be used to create transitional storage selections where all channels are enabled.
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51} . Maximum time is 9.007×10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
External Signal In ¹	A backplane input signal
External Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as External Signal In, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
MagniVu acquisition trigger	Triggering of MagniVu memory is controlled by the main acquisition trigger
MagniVu trigger position	The MagniVu trigger position is programmable within 4 ns boundaries and separate from the main acquisition memory trigger position.
Increment counter	Either of the two counter/timers used as counters can be incremented.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues from the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other instruments
Trigger out	A trigger out signal sent to the backplane to trigger other instruments

Table A-8: TLA600 trigger system (Cont.)

Characteristic	Description
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Not allowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 10 ns.
Setup and hold violation storage	The acquisition memory can be enabled to store setup and hold violation information with each data sample when synchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The maximum clock rate is reduced by half.

- ¹ Each use of External Signal In, glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.
- ² Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.
- ³ Any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns.

Table A-9: TLA600 MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory. There are no clocking options.

Table A-10: TLA600 Data handling

Characteristic	Description
Nonvolatile memory retention time (Typical)	Battery is integral to the NVRAM. Battery life is > 10 years.

Table A-11: TLA600 internal controller

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Celeron, 500 MHz
Main Memory	SDRAM
Style	168 pin DIMM, 2 Sockets
Speed	100 MHz
Installed Configurations	Minimum 64 MB loaded in one socket Maximum 128 MB with both sockets loaded
Real-Time Clock and CMOS Setups, Plug & Play NVRAM Retention Time	Battery life is typically > 3 years when the logic analyzer is not connected to line voltage. When connected to line voltage the life of the battery is extended. Lithium battery, CR3032
Hard Disk Drive	Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface.
Size	Minimum 10 GByte Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
CD ROM Drive	Standard PC compatible IDE (Integrated Device Electronics) 40X (minimum) CD ROM drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment.
Floppy Disk Drive	Standard 3.5 inch 1.44-MB PC compatible high-density, double-sided floppy disk drive.

Table A-12: TLA600 display system

Characteristic	Description																		
Classification	Standard PC graphics accelerator technology (bitBLT-based); capable of supporting both internal color LCD display and external color SVGA/XGA monitor																		
Display Memory Size	DRAM-based frame-buffer memory 2 MB																		
Display Selection	Both front panel and external displays can be used simultaneously, each with independent resolutions.																		
External Display Drive Display Size	One SVGA/XGA-compatible analog output port Selected via Windows Plug and Play support for DDC1 and DDC2 A and B <table border="0"> <thead> <tr> <th>Resolution (Pixels)</th> <th>Colors</th> </tr> </thead> <tbody> <tr> <td>640 x 480</td> <td>256</td> </tr> <tr> <td>640 x 480</td> <td>64,000</td> </tr> <tr> <td>640 x 480</td> <td>16,800,000</td> </tr> <tr> <td>800 x 600</td> <td>256</td> </tr> <tr> <td>800 x 600</td> <td>64,000</td> </tr> <tr> <td>800 x 600</td> <td>16,800,000</td> </tr> <tr> <td>1024 x 768</td> <td>256</td> </tr> <tr> <td>1280 x 1024</td> <td>256</td> </tr> </tbody> </table>	Resolution (Pixels)	Colors	640 x 480	256	640 x 480	64,000	640 x 480	16,800,000	800 x 600	256	800 x 600	64,000	800 x 600	16,800,000	1024 x 768	256	1280 x 1024	256
Resolution (Pixels)	Colors																		
640 x 480	256																		
640 x 480	64,000																		
640 x 480	16,800,000																		
800 x 600	256																		
800 x 600	64,000																		
800 x 600	16,800,000																		
1024 x 768	256																		
1280 x 1024	256																		
Internal Display Classification	Thin Film Transistor (TFT) 10.4 inch active-matrix color LCD display; CCFL backlight; intensity controllable via software																		
Resolution	800 x 600 pixels																		
Color Scale	262,144 colors (6-bit RGB)																		

Table A-13: TLA600 front-panel interface

Characteristic	Description
QWERTY Keypad	ASCII keypad to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
Special Function Knobs	Various functions

Table A-14: TLA600 rear-panel interface

Characteristic	Description
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM 1)	9-pin male sub-D connector to support RS-232 serial port
Single USB Ports	One USB (Universal Serial Bus) compliant port
SVGA Output Port (SVGA OUT)	15-pin sub-D SVGA connector
Mouse Port	PS/2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	PS/2 compatible keyboard port utilizing a mini DIN connector
Type I and II PC Card Port	Standard Type I and II PC-compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC-compatible PC card slot

Table A-15: TLA600 AC power source

Characteristic	Description
Source Voltage and Frequency	90–250 V _{RMS} , 45–66 Hz, continuous range CAT II 100–132 V _{RMS} , 360–440 Hz, continuous range CAT II
Fuse Rating	
90 V – 132 V Operation (2 required)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
90 V - 250 V Operation (2 required)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum Power Consumption	600 Watts line power maximum
Steady-State Input Current	6 A _{RMS} maximum
Inrush Surge Current	70 A maximum
Power Factor Correction	Yes
On/Standby Switch and Indicator	Front Panel On/Standby switch, with indicator. The power cord provides main power disconnect.

Table A-16: TLA600 cooling

Characteristic	Description
Cooling System	Forced air circulation (negative pressurization) utilizing six fans operating in parallel
Cooling Clearance	2 in (51 mm), sides and rear; unit should be operated on a flat, unobstructed surface

Table A-17: TLA600 mechanical characteristics

Characteristic	Description
Overall Dimensions	See Figure A-1 for overall chassis dimensions
Weight	Includes empty accessory pouch and front cover
TLA614, TLA624, TLA613, and TLA623	18.1 Kg (40 lbs)
TLA612, TLA622, TLA611, and TLA621	18 Kg (39.75 lbs)
TLA604 and TLA603	17.6 Kg (38.75 lbs)
TLA602 and TLA601	17.5 Kg (38.5 lbs)

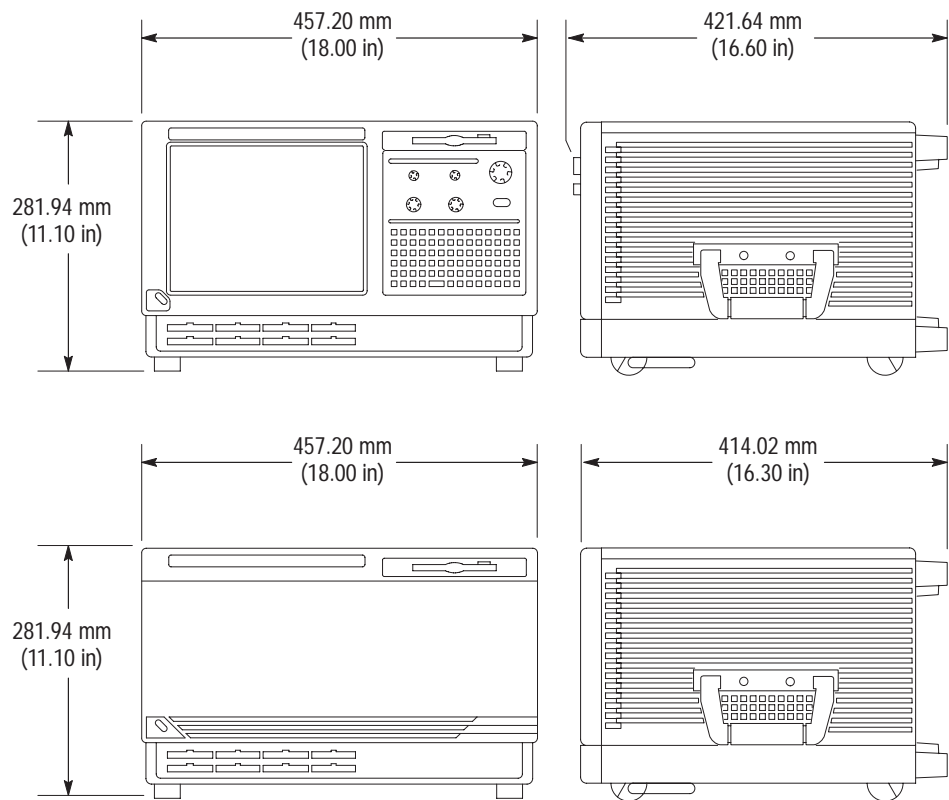


Figure A-1: Dimensions of the TLA600 series logic analyzer

TLA700 System Specifications

Tables A–18 through A–20 list the specifications common to the TLA714 and TLA720 logic analyzers. Detailed specifications for the TLA714 Color Portable Mainframe begin on page A–22. Detailed specifications for the TLA720 Benchtop Controller begin on page A–31.

Table A–18: TLA700 Backplane interface

Characteristic	Description
Slots	
Portable mainframe	4
Benchtop mainframe	13
Expansion mainframe	13
✓ CLK10 Frequency	10 MHz ±100 PPM
Relative Time Correlation Error ^{1,2} (<i>Typical</i>)	
LA to LA “MagniVu” data	2 ns
LA to LA “normal” data utilizing an internal clock	1 LA sample – 0.5 ns
LA to LA “normal” data utilizing an external clock	2 ns
LA “MagniVu” to DSO data	3 ns
LA to DSO “normal” data utilizing an internal clock ³	1 LA sample + 1 ns
LA to DSO “normal” data utilizing an external clock ³	3 ns
DSO to DSO ³	3 ns

¹ Includes typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a “typical” number for the measurement. Assumes standard accessory probes are utilized.

² For time intervals longer than 1 μs between modules, add 0.01% of the difference between the absolute time measurements to the relative time correlation error to account for the inaccuracy of the CLK10 source.

³ The DSO module time correlation is measured at the maximum sample rate on one channel only.

Table A–19: TLA700 Backplane latencies

Characteristic	Portable mainframe and Benchtop mainframe	Expansion mainframe
System Trigger and External Signal Input Latencies ^{2,3} (Typical)		
External System Trigger Input to LA Probe Tip ⁴	–266 ns	–230 ns
External Signal Input to LA Probe Tip via Signal 3, 4 ⁵	–212 ns + Clk	–176 ns + Clk
External Signal Input to LA Probe Tip via Signal 1, 2 ^{5, 6}	–208 ns + Clk	–187 ns + Clk
External System Trigger Input to DSO Probe Tip ⁴	–25 ns	–11 ns
System Trigger and External Signal Output Latencies ³ (Typical)		
LA Probe Tip to External System Trigger Out ¹	376 ns + SMPL	412 ns + SMPL
LA Probe Tip to External Signal Out via Signal 3, 4 ¹		
OR function	366 ns + SMPL	402 ns + SMPL
AND function	379 ns + SMPL	415 ns + SMPL
LA Probe Tip to External Signal Out via Signal 1, 2 ^{3,6}		
normal function	364 ns + SMPL	385 ns + SMPL
inverted logic on backplane	364 ns + SMPL	385 ns + SMPL
DSO Probe Tip to External System Trigger Out	68 ns	104 ns
DSO Probe Tip to External Signal Out via Signal 3, 4		
OR function	65 ns	101 ns
AND function	75 ns	111 ns
DSO Probe Tip to External Signal Out via Signal 1, 2 ⁶		
normal function	68 ns	89 ns
inverted logic on backplane	71 ns	92 ns
Inter-Module Latencies ³ (Typical)		
LA to DSO Inter-module System Trigger ^{1,4}	358 ns + SMPL	394 ns + SMPL
LA to LA Inter-module System Trigger ^{1,4}	66 ns + SMPL	102 ns + SMPL
LA to DSO Inter-Module ARM ¹	360 ns + SMPL	396 ns + SMPL
LA to LA Inter-Module ARM ^{1,5}	108 ns + SMPL + Clk	144 ns + SMPL + Clk
LA to LA Inter-Module via Signal 1, 2 ^{1,5, 6}	116 ns + SMPL + Clk	137 ns + SMPL + Clk
LA to LA Inter-Module via Signal 3, 4 ^{1,5}	116 ns + SMPL + Clk	152 ns + SMPL + Clk
DSO to DSO Inter-module System Trigger ⁴	50 ns	86 ns
DSO to LA Inter-module System Trigger ⁴	–240 ns	–204 ns
DSO to LA Inter-Module ARM ⁵	–192 ns + Clk	–156 ns + Clk
DSO to DSO Inter-Module ARM	59 ns	95 ns

Table A-19: TLA700 Backplane latencies (Cont.)

Characteristic	Portable mainframe and Benchtop mainframe	Expansion mainframe
DSO to LA Inter-Module via Signal 1, 2 ^{5, 6}	-179 ns + Clk	-158 ns + Clk
DSO to LA Inter-Module via Signal 3, 4 ⁵	-184 ns + Clk	-148 ns + Clk

- ¹ SMPL represents the time from the event at the probe tip inputs to the next valid data sample of the LA module. In the Normal Internal clock mode, this represents the delta time to the next sample clock. In the MagniVu Internal clock mode, this represents 500 ps or less. In the External clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.
- ² All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.
- ³ Latencies are based on typical portable mainframe configurations consisting of two LA modules or an LA module plus a DSO module. Latencies are system-configuration-dependent and may vary slightly with module loading.
- ⁴ In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.
- ⁵ "Clk" represents the time to the next master clock at the destination logic analyzer. In the asynchronous (or internal) clock mode, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. In the synchronous (or external) clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.
- ⁶ Signals 1 and 2 (ECLTRG0, 1) are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.

Table A-20: TLA700 External signal interface

Characteristic	Description
System Trigger Input	TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Input Levels V_{IH} V_{IL}	TTL compatible input $\geq 2.0\text{ V}$ $\leq 0.8\text{ V}$
Input Mode	Falling edge sensitive, latched (active low)
Minimum Pulse Width	12 ns
Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods
Maximum Input Voltage	0 to +5 V peak
External Signal Input	TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Input Destination	Signal 1, 2, 3, 4
Input Levels V_{IH} V_{IL}	TTL compatible input $\geq 2.0\text{ V}$ $\leq 0.8\text{ V}$
Input Mode	Active (true) low, level sensitive
Input Bandwidth ¹ Signal 1, 2 Signal 3, 4	50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Accepts signals during valid acquisition periods via real-time gating
Maximum Input Voltage	0 to +5 V peak
System Trigger Output	TTL compatible output via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Source Mode	Active (true) low, falling edge latched
Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output $\geq 4\text{ V}$ into open circuit $\geq 2\text{ V}$ into 50 Ω to ground $\leq 0.7\text{ V}$ sinking 10 ma
Output Protection	Short-circuit protected (to ground)
External Signal Output	TTL compatible outputs via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Source Selection	Signal 1, 2, 3, 4, or 10 MHz clock
Output Modes Level Sensitive	User definable Active (true) low or active (true) high

Table A-20: TLA700 External signal interface (Cont.)

Characteristic	Description
Output Levels V_{OH}	50 Ω back terminated TTL output ≥ 4 V into open circuit ≥ 2 V into 50 Ω to ground
V_{OL}	≤ 0.7 V sinking 10 ma
Output Bandwidth ² Signal 1, 2 Signal 3, 4	50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously
Output Protection	Short-circuit protected (to ground)
Intermodule Signal Line Bandwidth Signal 1, 2 (ECLTRG 0,1) Signal 3, 4 (ECLTRG 0,1)	Minimum bandwidth up to which the intermodule signals are specified to operate correctly 50 MHz square wave minimum 10 MHz square wave minimum

¹ The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

² The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

TLA714 Color Portable Mainframe Characteristics

Tables A–21 through A–28 describe the specifications for the TLA714 Color Portable Mainframe.

Table A–21: TLA714 Internal controller

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Pentium PC-AT configuration with a 266 MHz Intel Pentium MMX microprocessor
Main Memory	SDRAM
Style	144 pin SO DIMM, 2 Sockets
Speed	66 MHz
Installed Configurations	Minimum 64 MB loaded in one socket Maximum 128 MB with both sockets loaded
Cache Memory	512 KB Level 2 (L2) write-back cache
Flash BIOS	512 KB Provides PC plug-and-play services with and without Microsoft Windows operating system. Flash based BIOS field upgradable via a floppy disk.
Real-Time Clock and CMOS Setups NVRAM	Real-Time clock/calendar, with typical 10-year life. Standard and advanced PC CMOS setups.
Bootable Replaceable Hard Disk Drive	Standard PC compatible IDE (Integrated device Electronics) hard disk drive residing on an EIDE interface.
Size	Minimum 10 GByte Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
Interface	ATA 4/Enhanced IDE (EIDE)
Average seek time	Read 13 ms
I/O data-transfer rate	33.3 MB/s max (U-DMA mode 2) (ATA33)
CD ROM Drive	Standard PC compatible IDE (Integrated device Electronics) 24X (minimum) CD ROM drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment.
Floppy Disk Drive	Standard 3.5 inch 1.44-MB PC compatible high-density, double-sided floppy disk drive.

Table A-22: TLA714 display system

Characteristic	Description																				
Classification	Standard PC graphics accelerator technology (bitBLT-based); capable of supporting both internal color LCD display and external color SVGA/XGA monitor																				
Display Memory Size	DRAM-based frame-buffer memory 2 MB																				
Display Selection	Hardware sense of external SVGA monitor during BIOS boot sequence; defaults to internal color LCD display; automatically switches to external SVGA monitor, if attached Dual (simultaneous) display of external SVGA monitor and internal color LCD is possible via special "simulscan" CMOS setup, as long as internal and external displays operate at same resolution (limited to 800x600 on current TFT LCD) and display rates Dynamic Display Configuration (DDC2 A and B) support for external SVGA monitor is provided.																				
External Display Drive Display Size	One SVGA/XGA-compatible analog output port User selected via Microsoft Windows Plug and Play support for DDC1 and DDC2 A and B <table border="1"> <thead> <tr> <th>Resolution (Pixels)</th> <th>Colors</th> </tr> </thead> <tbody> <tr> <td>640 x 480</td> <td>256</td> </tr> <tr> <td>640 x 480</td> <td>64,000</td> </tr> <tr> <td>640 x 480</td> <td>16,800,000</td> </tr> <tr> <td>800 x 600</td> <td>256</td> </tr> <tr> <td>800 x 600</td> <td>64,000</td> </tr> <tr> <td>800 x 600</td> <td>16,800,000</td> </tr> <tr> <td>1024 x 768</td> <td>256</td> </tr> <tr> <td>1280 x 1024</td> <td>256</td> </tr> <tr> <td>1600 x 1200</td> <td>256</td> </tr> </tbody> </table>	Resolution (Pixels)	Colors	640 x 480	256	640 x 480	64,000	640 x 480	16,800,000	800 x 600	256	800 x 600	64,000	800 x 600	16,800,000	1024 x 768	256	1280 x 1024	256	1600 x 1200	256
Resolution (Pixels)	Colors																				
640 x 480	256																				
640 x 480	64,000																				
640 x 480	16,800,000																				
800 x 600	256																				
800 x 600	64,000																				
800 x 600	16,800,000																				
1024 x 768	256																				
1280 x 1024	256																				
1600 x 1200	256																				
Internal Display Classification	Thin Film Transistor (TFT) 10.4 inch active-matrix color LCD display; CCFL backlight; intensity controllable via software																				
Resolution	800 x 600 pixels																				
Color Scale	262,144 colors (6-bit RGB)																				

Table A-23: TLA714 front-panel interface

Characteristic	Description
QWERTY Keypad	ASCII keypad to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
HEX Keypad	HEX keypad supporting text entry functions
Special Function Knobs	Various functions
Integrated Pointing Device	GlidePoint touchpad
Dual USB Ports	Two USB (Universal Serial Bus) compliant ports
Mouse Port	PS/2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	PS/2 compatible keyboard port utilizing a mini DIN connector

Table A-24: TLA714 rear-panel interface

Characteristic	Description
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM A)	9-pin male sub-D connector to support RS-232 serial port
SVGA Output Port (SVGA OUT)	15-pin sub-D SVGA connector
Type I and II PC Card Port	Standard Type I and II PC-compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC-compatible PC card slot

Table A-25: TLA714 AC power source

Characteristic	Description
Source Voltage and Frequency	90–250 V _{RMS} , 45–66 Hz, continuous range CAT II 100–132 V _{RMS} , 360–440 Hz, continuous range CAT II
Fuse Rating	
90 V - 250 V Operation (159-0046-00)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
90 V - 250 V Operation (159-0381-00)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum Power Consumption	600 W line power maximum
Steady-State Input Current	6 A _{RMS} maximum
Inrush Surge Current	70 A maximum

Table A-25: TLA714 AC power source (Cont.)

Characteristic	Description
Power Factor Correction	Yes
On/Standby Switch and Indicator	Front Panel On/Standby switch, with LED indicator located next to switch The power cord provides main power disconnect.

Table A-26: TLA714 secondary power

Characteristic	Description			
✓ DC Voltage Regulation (Combined System, voltage available at each slot)	Voltage	Minimum	Nominal	Maximum
	+24 V	23.28 V	24.24 V	25.20 V
	+12 V	11.64 V	12.12 V	12.60 V
	+5 V	4.875 V	5.063 V	5.250 V
	-2 V	-2.10 V	-2.00 V	-1.90 V
	-5.2 V	-5.460 V	-5.252 V	-5.044 V
	-12 V	-12.60 V	-12.12 V	-11.64 V
	-24 V	-25.20 V	-24.24 V	-23.28 V

Table A-27: TLA714 cooling

Characteristic	Description
Cooling System	Forced air circulation (negative pressurization) utilizing six fans operating in parallel
Cooling Clearance	2 in (51 mm), sides and rear; unit should be operated on a flat, unobstructed surface
Slot Activation	Installing a module activates the cooling for the corresponding occupied slots by opening the air flow shutter mechanism. Optimizes cooling efficiency by only applying airflow to modules that are installed.

Table A-28: TLA714 mechanical

Characteristic	Description
Overall Dimensions	(See Figure A-2 for overall chassis dimensions.)
Height (with feet)	9.25 in (235 mm)
Width	17.0 in (432 mm)
Depth	17.5 in (445 mm)
Weight (Typical)	30 lbs 12 oz. (13.9 kg) with no modules installed, 2 dual-wide slot covers, and empty pouch
Shipping configuration (Typical)	88 lbs (26.3 kg) minimum configuration (no modules or probes), with all standard accessories 87 lb (39.5 kg) full configuration, with 2 TLA7P4 modules and standard accessories (including probes)

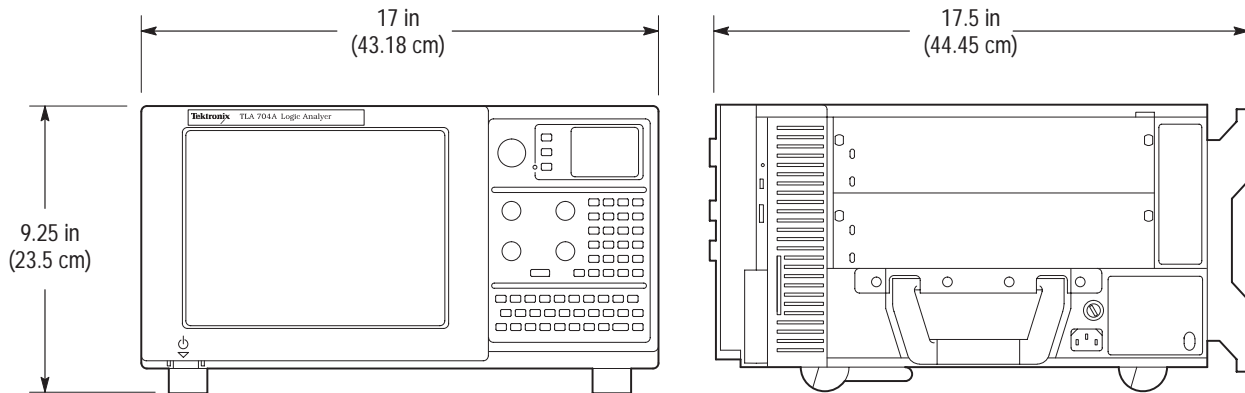


Figure A-2: Dimensions of TLA714 portable mainframe

Benchtop Chassis and Expansion Mainframe Characteristics

Tables A–29 through A–32 list the specifications for the TLA720 Benchtop chassis and the TL7XM expansion mainframe.

Table A–29: Benchtop chassis and expansion mainframe AC power source

Characteristic	Description
Source Voltage	90–250 V _{RMS} , 45–66 Hz, continuous range CAT II 100–132 V _{RMS} , 360–440 Hz, continuous range CAT II
Maximum Power Consumption	1450 W line power (the maximum power consumed by a fully loaded 13-slot instrument)
Fuse Rating (Current and voltage ratings and type of fuse used to fuse the source line voltage)	
90 V – 132 VAC _{RMS} Operation High-power/Low Line (159-0379-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: Slow acting Rating: 20 A/250 V
103 V – 250 VAC _{RMS} Operation (159-0256-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: No. 59/Fast acting Rating: 15 A/250 V
207 V – 250 VAC _{RMS} Operation (159-0381-00)	Safety: IEC 127/Sheet 1 Size: 5 mm × 20 mm Style: Fast acting "F", high-breaking capacity Rating: 6.3 A/250 V
Inrush Surge Current	70 A maximum
Steady State Input Current	16.5 A _{RMS} maximum at 90 VAC _{RMS} 6.3 A _{RMS} maximum at 207 VAC _{RMS}
Power Factor Correction	Yes
ON/Standby Switch and Indicator	Front Panel On/Standby switch with integral power indicator

Table A–30: Benchtop chassis and expansion mainframe secondary power

Characteristic	Description			
✓ DC Voltage Regulation (Combined System, voltage available at each slot)	Voltage	Minimum	Nominal	Maximum
	+24 V	23.28 V	24.24 V	25.20 V
	+12 V	11.64 V	12.12 V	12.60 V
	+5 V	4.875 V	5.063 V	5.250 V
	-2 V	-2.10 V	-2.00 V	-1.90 V
	-5.2 V	-5.460 V	-5.252 V	-5.044 V
	-12 V	-12.60 V	-12.12 V	-11.64 V
	-24 V	-25.20 V	-24.24 V	-23.28 V

Table A–31: Benchtop chassis and expansion mainframe cooling

Characteristic	Description
Cooling System	Forced air circulation system (positive pressurization) utilizing a single low-noise centripetal (squirrel cage) blower configuration with no filters.
Blower Speed Control	Rear panel switch selects between full speed and variable speed. Slot exhaust temperature and ambient air temperature are monitored such that a constant delta temperature is maintained across the module with the highest exit air temperature at the minimum operational blower speed.
Slot Activation	Installing a module activates the cooling for the corresponding occupied slots by opening the air flow shutter mechanism. Optimizes cooling efficiency by only applying airflow to modules that are installed.
Slot Airflow Direction	P2 to P1, bottom of module to top of module
Mainframe Air Intake	Lower fan-pack rear face and bottom
Mainframe Air exhaust	Top-sides and top-rear back. Top rear-back exhaust redirected to the sides by the fan pack housing to minimize reentry into the intake.
Δ Temperature Readout Sensitivity	100 mV/°C with 0°C corresponding to 0 V output
Temperature Sense Range	-10°C to +90°C, delta temperature \leq 50°C
Clearance	2 in (51 mm), rear, top, and sides

Table A-32: Benchtop chassis and expansion mainframe mechanical

Characteristic	Description
Overall Dimensions	(See Figures A-3 and A-4 for overall dimensions.)
Standard	
Height (with feet)	13.7 in (362.0 mm) including feet
Width	16.7 in (425.5 mm)
Depth	26.5 in (673.1 mm)
Rackmount	
Height	13.25 in (355.6 mm)
Width	18.9 in (480.1 mm)
Depth	28.9 in to 33.9 in (746.8 mm to 873.8 mm) in 0.5 in increments, user selectable
Weight	
Chassis with slot fillers (<i>Typical</i>)	52 lbs (23.6 kg)
Chassis with benchtop controller and slot fillers (<i>Typical</i>)	58 lbs 11 oz (26.6 kg)
Shipping configuration (<i>Typical</i>)	115 lbs (52.2 kg) minimum configuration with controller (or expansion module) and all standard accessories (no modules or probes) 187 lbs (84.8 kg) fully configured, 4 LA modules, 1 DSO modules, and all standard accessories including probes.
Rackmount kit adder	20 lbs (9.1 kg)
Module Size	13 plug-in slots

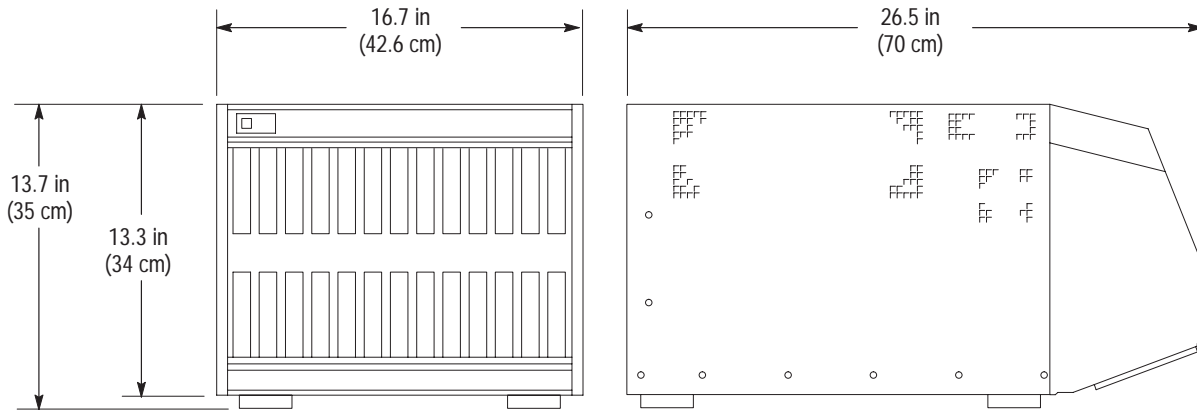


Figure A-3: Dimensions of the benchtop chassis and expansion mainframe

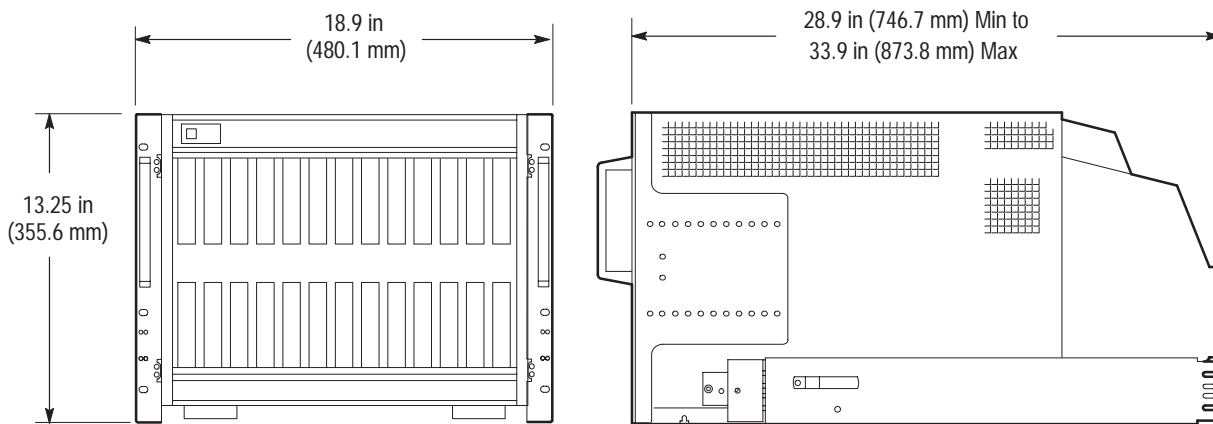


Figure A-4: Dimensions of the benchtop chassis and expansion mainframe with rackmount option

TLA720 Color Benchtop Controller Characteristics

Tables A–33 through A–34 list the specifications for the TLA720 Benchtop Controller.

Table A–33: Benchtop controller characteristics

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Pentium 266 MHz PC-AT configuration with an Intel chip-set
Main Memory	SDRAM
Style	Two 144 pin SODIMM sockets support one or two SDRAM modules
Installed Configuration	128 MB Two 64 MB SDRAM modules installed
Speed	60 ns
Cache Memory	256 K, level 2 (L2) write-back cache
Flash BIOS	512 KB Provides PC plug-and-play services with and without Microsoft Windows operating system. Flash based BIOS field upgradable via a floppy disk
Real-Time Clock and CMOS Setups NVRAM (Typical)	Real-time clock/calendar, with typical 7-year life. Standard and advanced PC CMOS setups: see BIOS specification. Year 2000 compliant.
Floppy Disk Drive	Standard 3.5 inch, 1.44 MB, double-sided, PC-compatible high-density floppy disk drive
Bootable Replaceable Hard Disk Drive	Standard PC compatible IDE (Integrated device Electronics) hard disk drive residing on an EIDE interface
Size	Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment These storage capacities valid at product introduction
Interface	ATA-4/Enhanced IDE (EIDE)
Average seek time	Read 13 ms
I/O data-transfer rate	33.3 MB/s maximum (U-DMA mode 2)
CD ROM Drive	Standard PC compatible IDE (Integrated device Electronics) 24X (minimum) CD ROM drive residing on an EIDE interface Continually subject to change due to the fast-moving PC component environment

Table A–33: Benchtop controller characteristics (Cont.)

Characteristic	Description
Display Classification	Standard PC graphics accelerator technology (bitBLT based) capable of driving external color VGA, SVGA, or XGA monitors
Display Memory	DRAM based frame-buffer memory
Size	2 MB
Display Drive	One VGA, SVGA, or XGA compatible analog output port
Display Size	User selected via Microsoft Windows
	Plug and Play support for DDC1 and DDC2 A and B
	Resolution (Pixels) Colors
	640 x 480 256
	640 x 480 64,000
	640 x 480 16,800,000
	800 x 600 256
	800 x 600 64,000
	800 x 600 16,800,000
	1024 x 768 256
	1280 x 1024 256
	1600 x 1200 256
SVGA Output Port (SVGA)	The SVGA port utilizing a 15-pin sub-D SVGA connector
Dual USB Ports	Two USB (Universal Serial Bus) compliant ports
Mouse Port	Front panel mounted PS2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	Front panel mounted PS2 compatible keyboard port utilizing a mini DIN connector
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM)	9-pin male sub-D connector to support an RS232 serial port
Type I and II PC Card Port	Standard Type I and II PC compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC compatible PC card slot

Table A–34: Benchtop controller mechanical characteristics

Characteristic	Description
Weight (<i>Typical</i>)	6 lb. 10 oz. (2.9 kg)
Size	Three slots wide
Overall dimensions	
Height	10.32 in (262 mm)
Width	3.6 in (83 mm)
Depth	14.7 in (373 mm)

LA Module Characteristics

Tables A–35 through A–41 list the specifications of the logic analyzer modules. The specifications apply to all versions of the logic analyzer module unless otherwise noted.

Table A–35: LA module channel width and depth

Characteristic	Description	
Number of channels	Product	Channels
	TLA7N1, TLA7L1, TLA7M1	32 data and 2 clock
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	64 data and 4 clock
	TLA7N3, TLA7L3, TLA7M3	96 data, 4 clock, and 2 qualifier
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	Product	Memory depth
	TLA7L1, TLA7L2, TLA7L3, TLA7L4	32 K or 128 K samples ¹
	TLA7M1, TLA7M2, TLA7M3, TLA7M4	512 K samples
	TLA7N1, TLA7N2, TLA7N3, TLA7N4	64 K or 256 K or 1 M or 4 M samples ¹
	TLA7P2, TLA7P4	16 M samples
	TLA7Q2, TLAQP4	64 M samples

¹ PowerFlex options

Table A–36: LA module clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period ¹	4 ns to 50 ms in a 1–2–5 sequence 2 ns in 2x Clocking mode	
✓ Minimum recognizable word ² (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417 or a P6418 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
Synchronous clocking		
Number of clock channels ³	Product	Clock channels
	TLA7N1, TLA7L1, TLA7M1	2
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	4
	TLA7N3, TLA7L3, TLA7M3	4
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	4

Table A–36: LA module clocking (Cont.)

Characteristic	Description
Number of qualifier channels	Product
	TLA7N1, TLA7L1, TLA7M1
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2
	TLA7N3, TLA7L3, TLA7M3
	Qualifier channels
	0
	0
	2
	4
✓ Setup and hold window size (data and qualifiers)	<p>Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns</p> <p>Maximum setup time = User interface setup time + 0.8 ns</p> <p>Maximum hold time = User interface hold time + 0.2 ns</p> <p>Maximum setup time for slave module of merged pair = User Interface setup time + 0.8 ns</p> <p>Maximum hold time for slave module of merged pair = User Interface hold time + 0.7 ns</p> <p>Examples: for a P6417 or a P6418 probe and user interface setup and hold of 2.0/0.0 typical:</p> <p>Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns</p> <p>Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns</p> <p>Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns</p>
Setup and hold window size (data and qualifiers) (Typical)	<p>Channel-to-channel skew (<i>typical</i>) + (2 x sample uncertainty)</p> <p>Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns</p>
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.5 ns (Ts) to –7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.
✓ Maximum synchronous clock rate ⁴	<p>200 MHz in full speed mode (5 ns minimum between active clock edges)</p> <p>100 MHz in half speed mode (10 ns minimum between active clock edges)</p>
Demux clocking	
Demux Channels TLA7N3, TLA7N4, TLA7P4, TLA7Q4, TLA 7L3, TLA 7L4, TLA 7M3, TLA 7M4	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)
TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA 7L1, TLA 7L2, TLA 7M1, TLA 7M2	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA7N2, TLA7P2, TLA7Q2, TLA 7L2, TLA 7M2 only A0(7:0) to D0(7:0) TLA7N2, TLA7P2, TLA7Q2, TLA 7L2, TLA 7M2 only
Time between DeMux clock edges ⁴ (Typical)	5 ns minimum between DeMux clock edges in full-speed mode 10 ns minimum between DeMux clock edges in half-speed mode
Time between DeMux store clock edges ⁴ (Typical)	10 ns minimum between DeMux master clock edges in full-speed mode 20 ns minimum between DeMux master clock edges in half-speed mode

Table A-36: LA module clocking (Cont.)

Characteristic	Description
Data Rate (Typical) TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA7N3, TLA7N4, TLA7P4, TLA7Q4,	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.
Clocking state machine	
Pipeline delays	Each channel group can be programmed with a pipeline delay of 0 through 3 active clock edges.

- ¹ It is possible to use storage control and only store data when it has changed (transitional storage).
- ² Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.
- ³ Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.
- ⁴ Full and half speed modes are controlled by PowerFlex options and upgrade kits.

Table A-37: LA module trigger system

Characteristic	Description										
Triggering Resources											
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: <table style="width: 100%; border: none;"> <tr> <td style="width: 50%;">16 word recognizers</td> <td style="width: 50%;">0 range recognizers</td> </tr> <tr> <td>13 word recognizers</td> <td>1 range recognizer</td> </tr> <tr> <td>10 word recognizers</td> <td>2 range recognizers</td> </tr> <tr> <td>7 word recognizers</td> <td>3 range recognizers</td> </tr> <tr> <td>4 word recognizers</td> <td>4 range recognizers</td> </tr> </table>	16 word recognizers	0 range recognizers	13 word recognizers	1 range recognizer	10 word recognizers	2 range recognizers	7 word recognizers	3 range recognizers	4 word recognizers	4 range recognizers
16 word recognizers	0 range recognizers										
13 word recognizers	1 range recognizer										
10 word recognizers	2 range recognizers										
7 word recognizers	3 range recognizers										
4 word recognizers	4 range recognizers										
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across all the modules; the master module contains the most-significant groups. The master module is to the left (lower-numbered slot) of a merged pair. The master module is in the center when three modules are merged. Slave module 1 is located to the right of the master module, and slave module 2 is located to the left of the master module.										
Glitch detector ^{1,2}	Each channel group can be enabled to detect a glitch										
Minimum detectable glitch pulse width (Typical)	2.0 ns (single channel with P6417 or a P6418 probe)										

Table A-37: LA module trigger system (Cont.)

Characteristic	Description
Setup and hold violation detector ^{1,3}	Each channel group can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector ^{1, 4}	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample.
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51} . Maximum time is 9.007×10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
Signal In 1	A backplane input signal
Signal In 2	A backplane input signal
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
Increment counter	Either of the two counter/timers used as counters can be incremented.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues in the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other modules
Trigger out	A trigger out signal sent to the backplane to trigger other modules

Table A-37: LA module trigger system (Cont.)

Characteristic	Description
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Block storage is disallowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 10 ns.

- ¹ Each use of a glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.
- ² Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.
- ³ For TLA7N1, TLA7N2, TLA7N3, TLA7N4, TLA7P2, TLA7P4, TLA7Q2, and TLA7Q4 Logic Analyzer modules, any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns. For TLA7L1, TLA7L2, TLA7L3, TLA7L4, TLA7M1, TLA7M2, TLA7M3, and TLA7M4 Logic Analyzer modules, any setup value is subject to variation of up to 1.6 ns; any hold value is subject to variation of up to 1.4 ns.
- ⁴ This mode can be used to create transitional storage selections where all channels are enabled.

Table A-38: LA module MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory.

Table A-39: LA module data handling

Characteristic	Description
Nonvolatile memory retention time (Typical)	Battery is integral to the NVRAM. Battery life is > 10 years.

Table A–40: LA module input parameters with probes

Characteristic	Description
✓ Threshold Accuracy	± 100 mV
Threshold range and step size	Setable from +5 V to –2 V in 50 mV steps
Threshold channel selection	16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).
✓ Channel-to-channel skew	≤ 1.6 ns maximum (When merged, add 0.5 ns for the slave module.)
Channel-to-channel skew (Typical)	≤ 1.0 ns typical (When merged, add 0.3 ns for the slave module.)
Sample uncertainty	
Asynchronous:	Sample period
Synchronous:	500 ps
Probe input resistance (Typical)	20 k Ω
Probe input capacitance: P6417, P6434 (Typical)	2 pF
Probe input capacitance: P6418 (Typical)	1.4 pF data channels 2 pF CLK/Qual channels
Minimum slew rate (Typical)	0.2 V/ns
Maximum operating signal	6.5 V _{p-p} –3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum
Probe overdrive: P6417, P6418 P6434	± 250 mV or $\pm 25\%$ of signal swing minimum required beyond threshold, whichever is greater ± 300 mV or $\pm 25\%$ of signal swing minimum required beyond threshold, whichever is greater ± 4 V maximum beyond threshold
Maximum nondestructive input signal to probe	± 15 V
Minimum input pulse width signal (single channel) (Typical)	2 ns
Delay time from probe tip to input probe connector (Typical)	7.33 ns

Table A-41: LA module mechanical

Characteristic	Description
Slot width	Requires 2 mainframe slots
Weight (Typical)	5 lbs 10 oz. (2.55 kg) for TLA7N4 and TLA7P4 8 lbs (3.63 kg) for TLA7N4 and TLA7P4 packaged for domestic shipping
Overall dimensions	
Height	262 mm (10.32 in)
Width	61 mm (2.39 in)
Depth	373 mm (14.7 in)
Probe cables	
P6417 length	1.8 m (6 ft)
P6418 length	1.93 m (6 ft 4 in)
P6434 length	1.6 m (5 ft 2 in)
Mainframe interlock	1.4 ECL keying is implemented

DSO Module Characteristics

Tables A–42 through A–46 list the specifications for the DSO Module.

Table A–42: DSO module signal acquisition system

Characteristic	Description		
✓ Accuracy, DC gain	±1.5% for full scale ranges from 20 mV to 100 V ±2.0% for full scale ranges <19.9 mV		
✓ Accuracy, internal offset ¹	<i>Full scale range setting</i>	<i>Offset accuracy</i>	
	10 mV – 1 V	±[(0.2% × offset) + 1.5 mV + (6% × full scale range)]	
	1.01 V – 10 V	±[(0.25% × offset) + 15 mV + (6% × full scale range)]	
	10.1 V – 100 V	±[(0.25% × offset) + 150 mV + (6% × full scale range)]	
✓ Analog bandwidth, DC–50 Ω coupled	<i>Full scale range setting</i>	<i>Bandwidth²</i>	
	10.1 V – 100 V	DC – 500 MHz (TLA7E1 and TLA7E2) DC – 500 MHz (TLA7D1 and TLA7D2)	
	100 mV – 10 V	DC – 1 GHz (TLA7E1 and TLA7E2) DC – 500 MHz (TLA7D1 and TLA7D2)	
	50 mV – 99.5 mV	DC – 750 MHz (TLA7E1 and TLA7E2) DC – 500 MHz (TLA7D1 and TLA7D2)	
	20 mV – 49.8 mV	DC – 600 MHz (TLA7E1 and TLA7E2) DC – 500 MHz (TLA7D1 and TLA7D2)	
	10 mV – 19.9 mV	DC – 500 MHz (TLA7E1 and TLA7E2) DC – 500 MHz (TLA7D1 and TLA7D2)	
Bandwidth, analog, selections	20 MHz, 250 MHz, and FULL on each channel		
Calculated rise time (<i>Typical</i>) ³ Typical full-bandwidth rise times are shown in the chart to the right	<i>Full scale range setting</i>	<i>TLA7E1 and TLA7E2</i>	<i>TLA7D1 and TLA7D2</i>
	10.1 V – 100 V	900 ps	900 ps
	100 mV – 10 V	450 ps	900 ps
	50 mV – 99.5 mV	600 ps	900 ps
	20 mV – 49.8 mV	750 ps	900 ps
	10 mV – 19.9 mV	900 ps	900 ps
Crosstalk (channel isolation)	≥300:1 at 100 MHz and ≥100:1 at the rated bandwidth for the channel's sensitivity (Full Scale Range) setting, for any two channels having equal sensitivity settings		
Digitized bits	8		

Table A-42: DSO module signal acquisition system (Cont.)

Characteristic	Description		
Effective bits, real time sampling (<i>Typical</i>)	<i>Input frequency</i>	<i>TLA7E1 and TLA7E2 5 GS/s (each channel)</i>	<i>TLA7D1 and TLA7D2 2.5 GS/s (each channel)</i>
	10.2 MHz	6.2 bits	6.2 bits
	98 MHz	6.1 bits	6.1 bits
	245 MHz	6.0 bits	6.0 bits
	490 MHz	5.7 bits	5.7 bits
	990 MHz	5.2 bits	N/A
Frequency limit, upper, 20 MHz bandwidth limited (<i>Typical</i>)	20 MHz		
Frequency limit, upper, 250 MHz bandwidth limited (<i>Typical</i>)	250 MHz		
Input channels	<i>Product</i>	<i>Channels</i>	
	TLA7E2	Four	
	TLA7D2	Four	
	TLA7E1	Two	
	TLA7D1	Two	
Input coupling	DC, AC, or GND ⁴		
Input impedance, DC-1 M Ω coupled	1 M Ω \pm 0.5% in parallel with 10 pF \pm 3 pF		
Input impedance selections	1 M Ω or 50 Ω		
Input resistance, DC-50 Ω coupled	50 Ω \pm 1%		
Input VSWR, DC-50 Ω coupled	\leq 1.3:1 from DC - 500 MHz, \leq 1.5:1 from 500 MHz - 1 GHz		
Input voltage, maximum, DC-1 M Ω , AC-1 M Ω , or GND coupled	300 V _{RMS} but no greater than \pm 420 V peak, Installation category II, derated at 20 dB/decade above 1 MHz		
Input voltage, maximum, DC-50 Ω or AC-50 Ω Coupled	5 V _{RMS} , with peaks \leq \pm 25 V		
Lower frequency limit, AC coupled (<i>Typical</i>)	\leq 10 Hz when AC-1 M Ω Coupled; \leq 200 kHz when AC-50 Ω Coupled ⁵		
✓ Random noise	<i>Bandwidth selection</i>	<i>RMS noise</i>	
	Full	\leq (350 μ V + 0.5% of the full scale Setting)	
	250 MHz	\leq (165 μ V + 0.5% of the full scale Setting)	
	20 MHz	\leq (75 μ V + 0.5% of the full scale Setting)	

Table A–42: DSO module signal acquisition system (Cont.)

Characteristic	Description				
Range, internal offset	<i>Full scale range setting</i>		<i>Offset range</i>		
	10 mV – 1 V		±1 V		
	1.01 V – 10 V		±10 V		
	10.1 V – 100 V		±100 V		
Range, sensitivity (full scale range), all channels	10 mV to 100 V ⁶				
Step response settling errors (<i>Typical</i>) ^{7, 8}	<i>Full scale range setting</i>	\pm <i>Step response</i>	<i>Maximum settling error (%) at</i>		
			<i>20 ns</i>	<i>100 ns</i>	<i>20 ms</i>
	10 mV – 1 V	≤2 V	0.5%	0.2%	0.1%
	1.01 V – 10 V	≤20 V	1.0%	0.5%	0.2%
	10.1 V – 100 V	≤200 V	1.0%	0.5%	0.2%

- ¹ Net offset is the nominal voltage level at the digitizing oscilloscope input that corresponds to the center of the A/D Converter dynamic range. Offset accuracy is the accuracy of this voltage level.
- ² The limits given are for the ambient temperature range of 0°C to +30°C. Reduce the upper bandwidth frequencies by 5 MHz for each °C above +30°C. The bandwidth must be set to FULL.
- ³ Rise time (rounded to the nearest 50 ps) is calculated from the bandwidth when Full Bandwidth is selected. It is defined by the following formula:

$$\text{Rise Time (ns)} = 450 \div \text{BW (MHz)}$$
- ⁴ GND input coupling disconnects the input connector from the attenuator and connects a ground reference to the input of the attenuator.
- ⁵ The AC Coupled Lower Frequency Limits are reduced by a factor of 10 when 10X passive probes are used.
- ⁶ The sensitivity ranges from 10 mV to 100 V full scale in a 1–2–5 sequence of coarse settings. Between coarse settings, you can adjust the sensitivity with a resolution equal to 1% of the more sensitive coarse setting. For example, between the 500 mV and 1 V ranges, the sensitivity can be set with 5 mV resolution.
- ⁷ The Full Bandwidth settling errors are typically less than the percentages from the table.
- ⁸ The maximum absolute difference between the value at the end of a specified time interval after the mid-level crossing of the step, and the value one second after the mid-level crossing of the step, expressed as a percentage of the step amplitude. See IEEE std. 1057, Section 4.8.1, *Settling Time Parameters*.

Table A-43: DSO module timebase system

Characteristic	Description	
Range, Extended Realtime Sampling Rate	5 S/s to 10 MS/s in a 1-2.5-5 sequence	
Range, Realtime Sampling Rate	<i>Products</i>	<i>Limits</i>
	TLA7E1 and TLA7E2	25 MS/s to 5 GS/s on all channels simultaneously in a 1-2.5-5 sequence
	TLA7D1 and TLA7D2	25 MS/s to 2.5 GS/s on all channels simultaneously in a 1-2.5-5 sequence
Record Length	512, 1024, 2048, 4096, 8192, and 15000	
✓ Long Term Sample Rate	±100 ppm over any ≥ 1 ms interval	

Table A-44: DSO module trigger system

Characteristic	Description	
✓ Accuracy (Time) for Pulse Glitch or Pulse Width Triggering	<i>Time Range</i>	<i>Accuracy</i>
	2 ns to 500 ns	±(20% of Setting + 0.5 ns)
	520 ns to 1 s	±(104.5 ns + 0.01% of Setting)
✓ Accuracy (DC) for Edge Trigger Level, DC Coupled	±((2% × Setting) + 0.03 of Full Scale Range + Offset Accuracy) for signals having rise and fall times ≥20 ns	
Range (Time) for Pulse Glitch and Pulse Width Triggering	2 ns to 1 s	
Range, Trigger Level	<i>Source</i>	<i>Range</i>
	Any Channel	±100% of full scale range
Range, Trigger Point Position	Minimum: 0% Maximum: 100%	
Resolution, Trigger Level	0.2% of full scale for any Channel source	
Resolution, Trigger Position	One Sample Interval at any Sample Rate	
Sensitivities, Pulse-Type Runt Trigger (<i>Typical</i>)	10% of full scale, from DC to 500 MHz, for vertical settings >100 mV full scale and ≤10 V full scale at the BNC input	
Sensitivities, Pulse-Type Trigger Width and Glitch (<i>Typical</i>)	10% of full scale for vertical settings >100 mV full scale and ≤10 V full scale at the BNC input	

Table A-44: DSO module trigger system (Cont.)

Characteristic	Description		
✓ Sensitivity, Edge-Type Trigger, DC Coupled	The minimum signal levels required for stable edge triggering of an acquisition when the trigger source is DC-coupled		
	<i>Products</i>	<i>Trigger Source</i>	<i>Sensitivity</i>
	TLA7E1 and TLA7E2	Any Channel	3.5% of Full Scale Range from DC to 50 MHz, increasing to 10% of Full Scale Range at 1 GHz
	TLA7D1 and TLA7D2	Any Channel	3.5% of Full Scale Range from DC to 50 MHz, increasing to 10% of Full Scale Range at 500 MHz
Sensitivity, Edge-Type Trigger, Not DC Coupled (<i>Typical</i>)	<i>Trigger Coupling</i>		<i>Typical Signal Level for Stable Triggering</i>
	AC		Same as the DC-coupled limits for frequencies above 60 Hz; attenuates signals below 60 Hz
	High Frequency Reject		One and one-half times the DC-coupled limits from DC to 30 kHz; attenuates signals above 30 kHz
	Low Frequency Reject		One and one-half times the DC-coupled limits for frequencies above 80 kHz; attenuates signals below 80 kHz
	Noise Reject		Three times the DC-coupled limits
Time, Minimum Pulse or Rearm, and Minimum Transition Time, for Pulse-Type Triggering (<i>Typical</i>)	For vertical settings >100 mV and ≤10 V at the BNC input		
	<i>Pulse Class</i>	<i>Minimum Pulse Width</i>	<i>Minimum Rearm Width</i>
	Glitch	1 ns	2 ns + 5% of Glitch Width Setting
	Width	1 ns	2 ns + 5% of Width Upper Limit Setting
Trigger Position Error, Edge Triggering (<i>Typical</i>)	<i>Acquisition Mode</i>		<i>Trigger Position Error</i> ¹
	Sample		±(1 Sample Interval + 1 ns)

¹ The trigger position errors are typically less than the values given here. These values are for triggering signals having a slew rate at the trigger point of ≥5% of full scale/ns.

Table A-45: DSO module front-panel connectors

Characteristic	Description
✓ Probe Compensator, Output Voltage The Probe Compensator output voltage in peak-to-peak Volts	0.5 V (base-top) \pm 1% into a \geq 50 Ω load

Table A-46: DSO module mechanical

Characteristic	Description	
Slot width	Requires 2 mainframe slots	
Weight (Typical)	<i>Products</i>	<i>Weight</i>
	TLA7D1 and TLA7E1	2.44 kg (5.38 lbs)
	TLA7D2 and TLA7E2	2.55 kg (5.63 lbs)
Shipping Weight (Typical)	<i>Products</i>	<i>Weight</i>
	TLA7D1 and TLA7E1	6.35 kg (14 lbs)
	TLA7D2 and TLA7E2	7.71 kg (17 lbs)
Overall Dimensions	Height: 262.05 mm (10.32 in)	
	Width: 60.66 mm (2.39 in)	
	Depth: 373.38 mm (14.70 in)	

TLA7PG2 Pattern Generator Module Characteristics

Tables A–47 through A–52 list the specifications for the pattern generator module. For information on the P6470 and P6471 pattern generator probes, refer to *P6470 & P6471 Pattern Generator Probe Instructions*.

Table A–47: PG module electrical specification, operational mode

Characteristic	Description	Description
Operational mode		
Normal	Pattern data output is synchronized by the internal/external clock input	
Step	Pattern data output is synchronized by the software command	
Output pattern		
✓ Maximum Operating Clock Frequency	134 MHz in Full Channel Mode 268 MHz in Half Channel Mode	
Pattern length	40 to 262,140 ($2^{18} - 4$) in Full Channel Mode (standard) 80 to 524,280 ($2^{19} - 8$) in Half Channel Mode (standard) 40 to 1,048,572 ($2^{20} - 4$) in Full Channel Mode (option 1M or PowerFlex upgrade) 80 to 2,097,144 ($2^{21} - 8$) in Half Channel Mode (option1M or PowerFlex upgrade)	
Number of channels	64 channels in Full Channel Mode 32 channels in Half Channel Mode The pattern memory for the following data channel will be shared with strobe control/internal inhibit control	
	<i>Probe D data output channel</i>	<i>Control</i>
	D0:0	STRB0
	D0:1	STRB1
	D0:2	STRB2
	D0:3	STRB3
	D0:4	Inhibit probe A
	D0:5	Inhibit probe B
	D0:6	Inhibit probe C
	D0:7	Inhibit probe D
Sequences	Maximum 4,000	
Number of blocks	Maximum 4,000	
Number of subsequences	Maximum 50	
Subsequences	Maximum 256 steps	
Repeat count	1 to 65,536 or infinite	

Table A-48: PG module clocking

Characteristic	Description
Internal clock	
Clock Period	2.0000000 s to 7.462865 ns in Full Channel Mode 1.0000000 s to 3.7313432 ns in Half Channel Mode
Period Resolution	8 digits
Frequency Accuracy	± 100 PPM
External clock input	
Clock Rate	DC to 134 MHz in Full Channel Mode DC to 267 MHz in Half Channel Mode
Polarity	Normal or Invert
Threshold	
Range	-2.56 V to +2.54 V
Resolution	20 mV
Input Impedance	1 k Ω terminated to GND
Sensitivity	500 mV _{p-p}

Table A-49: PG module event processing

Characteristic	Description
Event Action	Advance, Jump and Inhibit
Number of Event Inputs	8 External Event Inputs (2 per each probe)
Number of Event Definitions	8 (A maximum of 256 event input patterns can be OR'd to define an event)
Event Mode	
for Advance	Edge or Level
for Jump	Edge or Level
Event Filter	None or 50 ns

Table A-50: PG module inter-module interactions

Characteristic	Description
Signal Input	Input from backplane Selectable from Signal 1, 2, 3, and 4 Used to define the Event
Signal Output	Output to backplane Selectable from Signal 1, 2, 3, and 4 Specified as High or Low in each Sequence line

Table A-51: PG module merged PG modules

Characteristic	Description
Number of modules that can be merged together	5
External Event Input for merged module	For Jump and Advance, only the External Event Input of the leftmost module is used. For Inhibit, each module uses its own External Event Input as a source

Table A-52: PG module mechanical

Characteristic	Description
Slot width	Requires 2 mainframe slots
Weight (Typical)	2.5 kg (5 lbs. 4 oz.)
Overall dimensions (excluding connectors)	
Height	10.32 in (262 mm)
Width	2.39 in (61 mm)
Depth	14.7 in (373 mm)
Mainframe interlock	1.4 ECI keying is implemented

Appendix B: TLA Symbol File Format

The logic analyzer can extract range symbol information directly from object files. The following are some of the formats. Check with your Tektronix representative for a complete listing of available formats.

OMF51, OMF86, OMF166, OMF286, OMF386, IEEE695, COFF, ELF/DWARF1 and DWARF2, and ELF/STABS

Users whose code generation tools do not generate these file formats can use TLA Symbol File (TSF) format (a text format). The TSF format is used by the logic analyzer when it exports symbol files. The logic analyzer can also read files in this format.

TLA symbol files consist of alphanumeric symbol names and associated data values. The files contain a header line and lines defining the symbol names and values. Fields on a line are separated with white space (blank spaces or tabs). The formats for the pattern symbol files and the various range symbol files differ; if you need to use pattern symbols and range symbols, use separate files.

Both TLA range and pattern symbol files have a .tsf file name extension (filename.tsf).

The first few lines of a TSF symbol file are typically comment lines describing when and how the file was generated.

```
# TLA Symbol File
# Created on Friday, May 29, 1998 at 09:52:03
# From file: "c:\quickstart\tla7qs.x"
```

All lines in a TSF file that begin with a number sign (#) character are treated as comments, unless the very next character is a plus sign (+). The plus sign signifies a file reader directive. (An example of a file reader directive “#+” can be seen in the TSF header definition on the next page.) The number sign character can also initiate a comment on the end of a symbol definition or other uncommented lines. All text between the number sign and the end of the line is treated as a comment and ignored.

TSF Headers

A TSF header identifies the file format version to potential file readers. It specifies whether the file contains pattern or range symbols, the radix used to specify symbol values, and an optional offset amount to be added to each symbol value (for range symbol files).

The TSF Header is a file directive which means that the following information begins with the special character combination of a number sign character followed immediately by a plus sign (#+). This is not a comment line. The special character sequence is used to mark instructions to the file reader; these instructions are called file directives.

The following examples show sample file headers for a pattern symbol file and a range symbol file. The first two lines are comments included for readability; they are not required as part of the file header.

```
#      TSF Format      Type      Display Radix  File Radix
# =====
#+ Version 2.1.0     PATTERN      HEX          HEX

#      TSF Format      Type      Display Radix  File Radix  Offset
# =====
#+ Version 2.1.0     RANGE        HEX          HEX          00000000
```

The File Format Version number contains three fields. The first two fields are the format major and minor version numbers. The logic analyzer will only read TSF files where the major and minor version number of the file is less than or equal to that of the TLA TSF symbol file reader. The third field is used to denote minor format changes which do not impact the file reader.

The File Format Version number is followed by a key word, PATTERN or RANGE, which signifies the type of symbols to be found in the file. TSF files can contain either type of symbols, but no single file can contain both. The header specifies the type for all symbols in the file.

The Display Radix field sets the default radix that will be used to display the numeric symbol value. For range symbol files this field must be one of the key words: HEX, DEC, OCT, or BIN. For pattern symbol files, only the key words: HEX, OCT, or BIN are allowed.

The File Radix field specifies the radix used by the symbol values in this file. Like the Display Radix field, the File Radix field must be one of the key words: HEX, DEC, OCT, or BIN for range symbol files, or HEX, OCT, or BIN for pattern symbol files.

The Offset field specifies an offset value and is applicable only to range symbol files. The offset value is specified in the radix indicated by the File Radix field. This offset value will be added to the lower and upper bounds of each range symbol that is read from the file. The offset is a 32-bit value, so it can have any value between 0x00000000 and 0xFFFFFFFF. If the sum of the offset and a range symbol bound value exceeds the 32-bit limit of 0xFFFFFFFF, the overflow bit is discarded. Negative offsets are specified by using a twos complement value for the offset.

TSF Pattern Symbols

Each pattern symbol in a TSF pattern file consists of two fields. The first field is the symbol name, and the second is the symbol pattern. The symbol name is a sequence of ASCII characters of up to 220 characters in length, although it is impractical to display symbol values much longer than 32 characters. Symbol names longer than 220 characters will be truncated during loading. The characters in a symbol name can be any character with an ASCII value between 0x21 (the exclamation point character, !) and 0x7E (the tilde character, ~). You can use symbol names with embedded spaces by enclosing the Symbol Name in double quotes.

# Symbol	Symbol	Optional Foreground
# Name	Pattern	and Background Color
# =====	=====	=====
NUL	X0000000	
SOH	X0000001	@red @yellow
STX	X0000010	
"ETX 0x03"	X0000011	

The symbol pattern consists of numerals in the radix specified by the File Radix field in the header, and Xs signifying “don’t-care” values. The number of bits represented by each character position in the pattern depends on the selected radix. For a radix of HEX, each character represents 4 bits. For an OCT radix, each character represents 3 bits; and for a BIN radix, each character represents one bit.

Symbol order in a TSF pattern file is important. When selecting the symbol to display for a particular value, the logic analyzer scans the list of pattern symbols from top to bottom. It selects the first symbol for which all non-don’t-care bits of the symbol match the corresponding bits of the target symbol.

TSF Range Symbols

There are four different types of range symbols:

- Function
- Variable
- Source
- Color

Each of these types define a range of 32-bit addresses associated with some entity.

Function range symbols define the beginning and ending addresses where instructions that implement a function are located in memory.

Variable range symbols define the beginning and ending addresses where the value of a variable is located in memory.

Source range symbols are similar to function range symbols, except that the address range for a source symbol describes the location of the instructions that implement just one source statement. (Source symbols also contain file name, line number, and an optional column range that define the location of the source code associated with the symbol.)

Color range symbols define a display color for any value that falls within a range.

Each of the types of range symbols appear in a separate section of the file. Each section begins with a file directive indicating the type of symbols that follow. The sections may appear in any order, and can be broken up and separated by other sections if necessary.

The first section might be variables, followed by functions, then followed by another variable section. Each section is also optional, however some logic analyzer applications are unable to use the symbol file if the appropriate type of symbols are not present. For example, the source window is only able to correlate with a listing window if the symbol file contains source symbols.

Range symbol names follow the same rules as pattern symbol names. The symbol name is a sequence of ASCII characters of up to 220 characters in length, even though it is impractical to display symbol values much longer than 32 characters.

Symbol names longer than 220 characters will be truncated during loading. The characters in a symbol name can be any character with an ASCII value between 0x21 (the exclamation point character, !) and 0x7E (the tilde character, ~). You can use symbol names with embedded spaces by enclosing the Symbol Name in double quotes.

Range symbol address ranges can overlap. This overlap sometimes produces unexpected results. When overlaps occur, and the logic analyzer needs to convert a numeric value to a symbol, it must choose between the overlapping symbols. When choosing between overlapping symbols, the logic analyzer assigns a precedence order to the symbol types. Function symbols have the highest precedence, followed by variable symbols, and then source symbols.

TSF Function Symbols

The file directive “#+ Function” introduces the function symbol section of a TSF Range file. The file directive tells the file reader that the following symbols represent functions, as opposed to variables or source statements. If no symbol type file directive is given, the function symbol type is assumed.

```
#+ Function
#           Symbol Name           Low      High
# =====
displayBanner      006035ba 00603675
buildMenus         00603676 006036e5
displayLCDmenu     006036e6 0060372f
```

Function symbols consist of three fields: the symbol name, the lower bound, and the upper bound.

The lower and upper bound values are each 32-bit values, defined by numerals in the radix specified by the File Radix field in the file header. These values define the lower and upper limits of the range of addresses occupied by the instructions which implement a function. Both values are inclusive, which means that the specified range includes both of the bound values, as well as all of the addresses between them.

TSF Variable Symbols

The file directive “#+ Variable” introduces the variable symbol section of a TSF Range file. The file directive tells the file reader that the following symbols represent variables, as opposed to functions or source statements. If no symbol type file directive is given, the function symbol type is assumed.

```
#+ Variable
#           Symbol Name           Low      High
# =====
menu         00000100 00000102
userMenu1   000004c0 000004c2
binBits     000004d4 000004d6
```

Variable symbols consist of three fields: the symbol name, the lower bound, and the upper bound. Variable symbols are just like function symbols except that they define the address range occupied by a variable, instead of function. The lower and upper bound values of a variable symbol are inclusive, meaning that they are themselves a part of the range. For variables occupying only a single byte in memory, the lower and upper bound values are equal.

TSF Source Symbols

The file directive “#+ Source” introduces the source symbol section of a TSF range file. The file directive tells the file reader that the following symbols represent source statements, as opposed to functions or variables. The source file directive must be followed by a file name, which specifies the name of the source file containing the following source statements. Each new set of symbols for a unique source file must be introduced with an additional source file directive to specify the file name for those symbols. If no symbol type file directive is given, the function symbol type is assumed.

```

#+ Source stoplite
# Line   Low      High     Beg End  Symbol Name
# =====
  27 006043ec 006043ef  0 25 # stoplite_27_25
  35 006043f0 006043f5  0 23 # stoplite_35_23
  47 006043f6 006043ff  0 30 # stoplite_47_30
  48 00604400 00604409  0 30 # stoplite_48_30
  49 0060440a 00604413  0 30 # stoplite_49_30
  50 00604414 0060441d  0 30 # stoplite_50_30
  51 0060441e 00604427  0 30 # stoplite_51_30
  52 00604428 00604431  0 30 # stoplite_52_30
  56 00604432 00604437  0 17 # stoplite_56_17
  59 00604438 00604439  0 18 # stoplite_59_18
  60 0060443a 00604445  0 37 # stoplite_60_37
  61 00604446 0060444d  0 33 # stoplite_61_33
  59 0060444e 0060444f  35 39 # stoplite_59_35
  59 00604450 00604455  19 34 # stoplite_59_19
  71 00604456 00604457  0 37 # stoplite_71_37
  74 00604458 0060445f  0 35 # stoplite_74_35
  77 00604460 00604467  0 36 # stoplite_77_36
  80 00604468 0060446f  0 36 # stoplite_80_36
  83 00604470 0060447b  0 43 # stoplite_83_43
  87 0060447c 00604483  0 34 # stoplite_87_34
  71 00604484 0060448d  0 37 # stoplite_71_37
  84 0060448e 00604490  0 29 # stoplite_84_29
    
```

The source symbols section consists of five fields for each source statement: line number, lower address bound, upper address bound, beginning column value, and ending column value.

Source symbols do not have a name in the same sense as function or variable symbols, because there is no name associated with each of the executable statements in a source file. Instead, a source symbol has a file name, specified in the source directive, and a line number. The line number specifies the line of the source file that contains the source statement. Line numbers are always in decimal regardless of the file radix in the header.

The lower and upper bound values for a source symbol are similar to those of function and variable symbols. For source symbols, these bounds represent the range of addresses occupied by the instructions that implement a single source statement.

The bound values are defined in the file radix specified in the header and can range in value from 0x00000000 to 0xFFFFFFFF. The lower and upper bound addresses are inclusive, just like other symbols. A source symbol for an instruction occupying a single memory location has matching lower and upper bound values.

The beginning and ending column fields of a source statement are optional. When present, and non-zero, they define the beginning and ending column position for the source statement.

The beginning and ending column values define the location of the statement in the line. This is especially useful when there are multiple statements on a single line, because it makes it possible to define a separate symbol for each statement. When the column information is not present, or is set to zero, the symbol is assumed to correspond to the entire line.

Only a few compilers generate column information, but when the information is present in the symbol file, the logic analyzer uses the column information to provide highly accurate source code correlation. The example source symbols on the previous page show typical column values.

In most cases only one of the column values is non-zero. This is because those lines contain only one statement, and the compiler specified only the column at which the statement ended. Some compilers specify only the beginning column position for such lines, in which case the beginning value would be non-zero and the ending value zero.

Note that there are three symbols corresponding to line 59 of the file. Line 59 of the original source file contains the following statement:

```
for (i = 0; i < NUM_STATES; i++)
```

This one line contains three separate statements. The first statement is the initialization (`i = 0`), the second statement is the test (`i < NUM_STATES`), and the third statement is the increment (`i++`).

Although all three statements appear on the same line, each generates a separate set of instructions, and the symbols in the example define unique address ranges for each. This enables the Source window to accurately indicate which of the three statements on the line is associated with any given address.

Each of the source symbols in the example includes a comment at the end of the line showing a symbol name. Since this is a comment, it is ignored by the symbol file reader, and is optional. When symbol files are exported by the logic analyzer, they contain comments that show the derived symbol name created by the logic analyzer itself. The name is a concatenation of the symbol file name, line number, and column number (if present). This is the symbol value that the logic analyzer will display for addresses that fall within the lower and upper bounds of a source symbol.

TSF Color Symbols

Color range symbols define the beginning and ending group values where a color is displayed. Any group value in the acquisition falling within this range will be shown in the defined color. The value range of a color symbol can overlap with the set of ranges defined by one or more Function, Variable, or Source symbols. In many instances a Color symbol will use exactly the same range bounds as a Function or Variable symbol.

A partial range file with colors is shown below:

```
#+ Color
#           Color                Low      High
# =====
@magenta   006035ba 00603640
@yellow @navy 00603541 00603675
@default @green 006036e6 0060372f
```

The first line tells the file reader that the following symbols represent colors. The next two lines are comments used as headers. The first color name specifies the foreground color, and the second optional color name specifies the background color. The available color names (keywords) are:

@black, @blue, @cyan, @lime, @magenta, @red, @yellow, @white,
@navy, @teal, @green, @purple, @maroon, @olive, @gray, and @silver.

The special color name @default gives the default text coloring specified by choosing a color in the Column tab of the Listing Window Property Sheet or the Waveform tab of the Waveform Window Property Sheet.

The Low and High columns describe the lower and upper bounds. The bounds are expressed as 32-bit values; the radix is specified in the header. The bounds are inclusive; the specified range includes both bound values, as well as all values between the bounds.

There is a different TSF symbol file syntax for adding color to range and pattern symbol files. For pattern symbol files, color is an attribute of existing pattern symbols. It is placed on the same line as the rest of the symbol, and to the right of the pattern definition. For range symbol files, color symbols are added in a separate section of the symbol file, just like Function, Variable, and Source

symbols. This allows the color information to be independent of the other defined range symbols.

A partial TSF Pattern Symbols file is shown below:

```
# Symbol Name      Pattern      Color
# =====      =====      =====
NUL                X000 0000
SOH                X000 0001   @blue
STX                X000 0010   @white @red
SBZ                X000 0100   @default @teal
```

Each Pattern symbol in a TSF Pattern file, consists of three fields. The first field is the Symbol Name, the second is the Symbol Pattern, and the third is Symbol Color.

The Symbol Color specification may contain zero, one, or two color keywords. If only one color is given, it specifies the foreground color of the data. If two colors are given, they specify the foreground color followed by the background color.

To supply a background color, you must give a foreground color. If you want to use the group's defined color from the Column or Waveform Property Page, you can use @default as the foreground color.

Appendix C: Pattern Generator Physical-Logical Conversion

The logic analyzer and DSO modules handle signals 1, 2, 3, and 4 with a logical expression (True/False). However, the pattern generator module handles these signals with a physical expression (High/Low). Select whether to use the signals as AND or OR from the TLA application's Signals property page of the System Configuration window. Use Tables C-1 and C-2 to convert physical expressions to logical expressions or vice versa.

Table C-1: For Signal 1, 2, and 3, 4, (logical function AND)

LA/DSO expression	Logical True	Logical False
Pattern generator signal output	High	Low
Pattern generator event definition	1	0

Table C-2: For Signal 3, 4 (logical function OR)

LA/DSO expression	Logical True	Logical False
Pattern generator signal output	Low	High
Pattern generator event definition	0	1

Only one module in the system can drive Signal 1. Only one module in the system can drive signal 2. When used with an expansion mainframe, all modules which drive Signal 3 should be in the same mainframe, and all modules which drive Signal 4 should be in the same mainframe.

Appendix D: TLA700 Module Installation

This section describes the steps to install modules in your TLA700 Series Logic Analyzer for the first time. It is written from the perspective that you purchased most of the items uninstalled and you intend to install all of the different items.



CAUTION. Do not install or remove any modules while the instrument is powered on, doing so can damage the modules or the mainframe.

Always power down the instrument before removing or inserting modules.

If your instrument does not have the modules preinstalled, the following is a suggestion to take advantage of airflow cooling.

Setting the Logical Address

Every module in the instrument must have a unique logical address; no two modules can have the same address. Two rotary switches on the rear panel select the logical address. Although Figure D-1 shows an LA module, the address switches are identical for all TLA modules. Read the following descriptions before changing the logical address.

NOTE. Do not set any module to logical address to 00. Logical address 00 is reserved exclusively for the controller.

Dynamic Logical Address Auto Configuration

The factory default switch setting is FF (Dynamic Auto Configuration). With dynamic logical address auto configuration selected, the instrument automatically sets the address to an unused value. For example, if there are modules set to addresses 01 and 02 already in your system, the resource manager will automatically assign the module an address other than 01 or 02. This allows you to freely move the modules around without reconfiguring the logical address.

Static Logical Address

Static logical address selections set the address to a fixed static logical address value. You can select any static addresses between 01 and FE hexadecimal (1 to 254 decimal). If you set the logical address switches to any other setting than FF, you must verify that no two modules (or devices) share the same address.

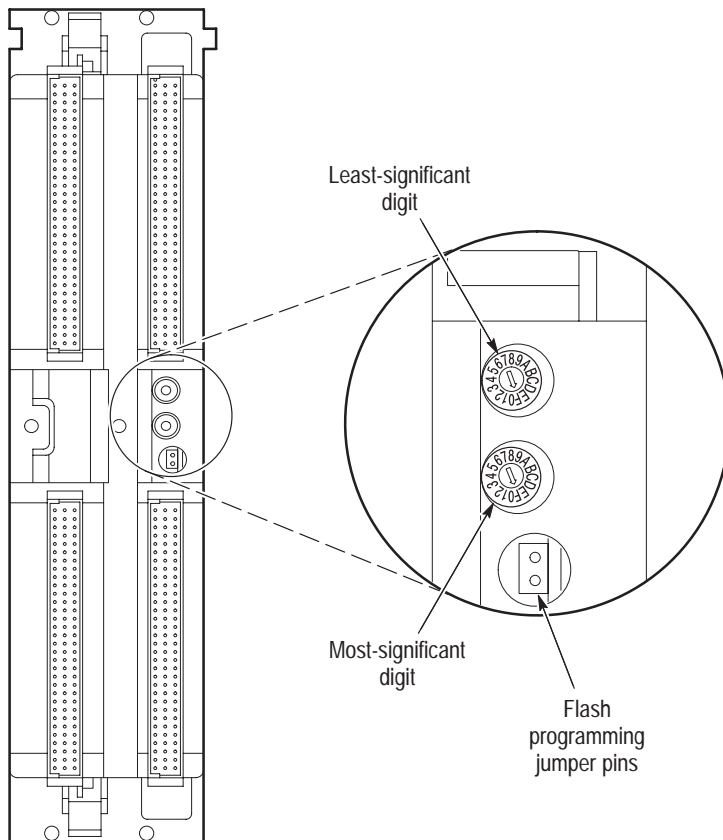


Figure D-1: Logical address switches

Module Address Problems

All modules are shipped with the logical address switch set to FF. This includes the fan controller board (located in the benchtop mainframe) which also requires a unique logical address.

If two modules (including the fan controller board) are set to the same address, the system will not work properly. The most common symptom of conflicting logical addresses is that a module will not show up in the system window.

Merging Modules

You can merge individual logic analyzer and pattern generator modules to create wider modules. Logic analyzer modules must be physically merged together by a merge cable and through software. Refer to *Appendix E: Merging Modules* for more information on merging modules.

Installing Modules in the Portable Mainframe

You can install any of the modules in any slot that the module key will allow; see Figure D-3. If you intend to merge the modules, disregard the following suggestions and refer to the merging modules rules on page E-1. If you are not merging the modules, and for air flow considerations, you should follow these guidelines:

- If a single LA module is to be installed, install it in slots 3-4. Place a double width slot cover over slots 1-2.
- If an LA module is to be installed with a DSO module, install the DSO module in slots 1-2, and the LA module in slots 3-4.
- If two LA modules are to be installed, install the module with the highest channel count in slots 1-2. Install the module with the lower channel count in slots 3-4.
- If two LA modules are to be installed, install the module with the largest memory in slots 3-4. Install the module with the lower memory in slots 1-2.

Use a screwdriver to tighten the retaining screws to 2.5 in-lbs after seating the modules in place. See Figure D-2.

Installing Modules in the Benchtop or Expansion Mainframes

You must install the benchtop controller in the benchtop mainframe in slots 0-2 (the TLA7XM Expansion Module must be located in slot 0). You can install any of the modules in any slot that the module key will allow; see Figure D-3.

If you intend to merge the modules, disregard the following suggestions and refer to the merging modules rules on page E-1. If you are not merging the modules, and for air flow considerations, you should follow these guidelines:

- If a single LA module is to be installed, install it in slots 3-4. Place a double width slot cover over slots 5-6, 7-8, 9-10 and 11-12.
- If an LA module is to be installed with a DSO module, install the LA module in slots 3-4, and the DSO module in slots 5-6. Place double width slot covers over slots 7-8, 9-10 and 11-12.
- If two or more LA modules are to be installed, install the module with the highest channel count in slots 3-4. Install the module with the lower channel count in slots 5-6. Place double width slot covers over slots 7-8, 9-10 and 11-12.
- If two or more LA modules are to be installed, install the module with the largest memory in slots 3-4. Install the module with the lower memory in slots 5-6. Place double width slot covers over slots 7-8, 9-10 and 11-12.

Use a screwdriver to tighten the retaining screws to 2.5 in-lbs after seating the modules in place. See Figure D-2.

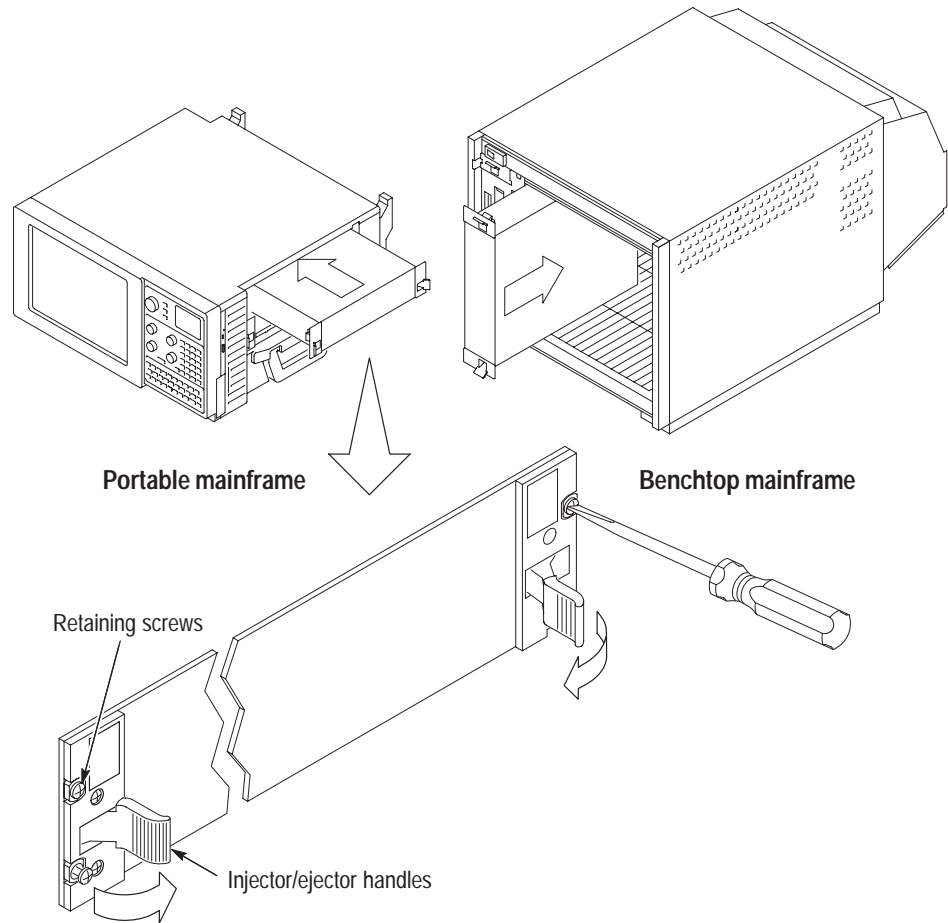


Figure D-2: Installing modules

Module Keying

Each module has a key that only allows certain modules to be installed next to other modules. For example, you can install a TLA7Dx DSO module to the left of a TLA7XM Expansion module, but you can not install a TLA7Nx LA module to the immediate left of a TLA7XM Expansion module. See Figure D-3.

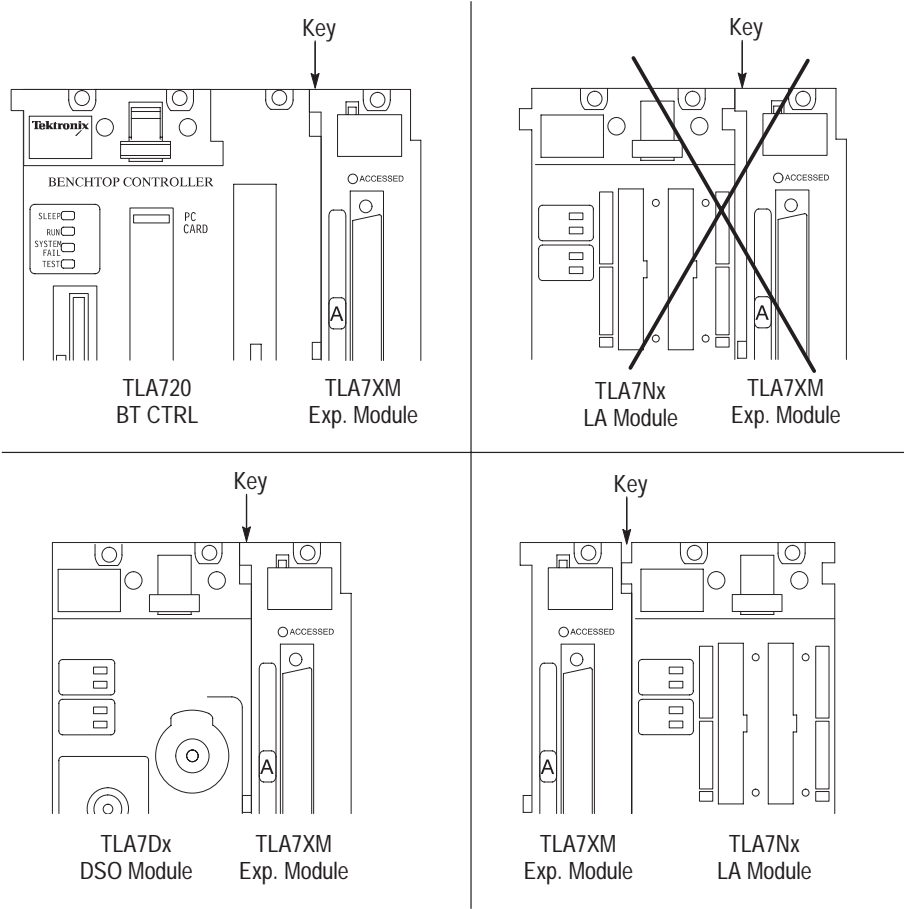


Figure D-3: Module keying

Covering Empty Slots

If you have any unused (empty) slots in your mainframe, you must install blank slot panel covers to meet EMC specifications. Install a blank slot panel cover for each empty slot as shown in Figure D-4 or D-5.

Make sure that the EMI shielding is in contact with the adjacent panel or module cover, and that the airflow shutter activation arms protrude through the holes in the blank shield.



CAUTION. Use only Tektronix TLA slot panel covers on the benchtop mainframe. Do not use non-Tektronix covers, otherwise the mainframe may not meet cooling and EMC requirements.

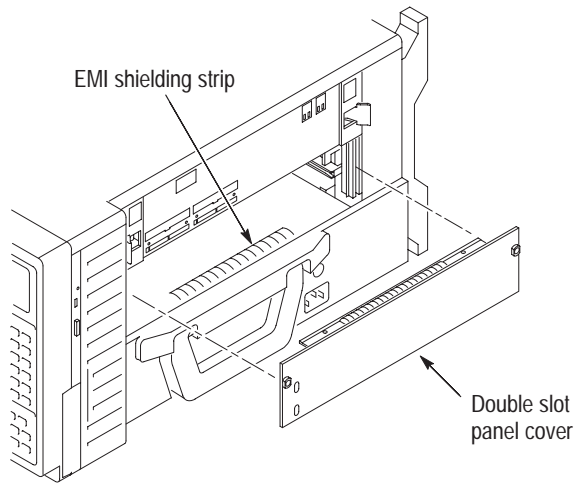


Figure D-4: Installing panel covers on the portable mainframe

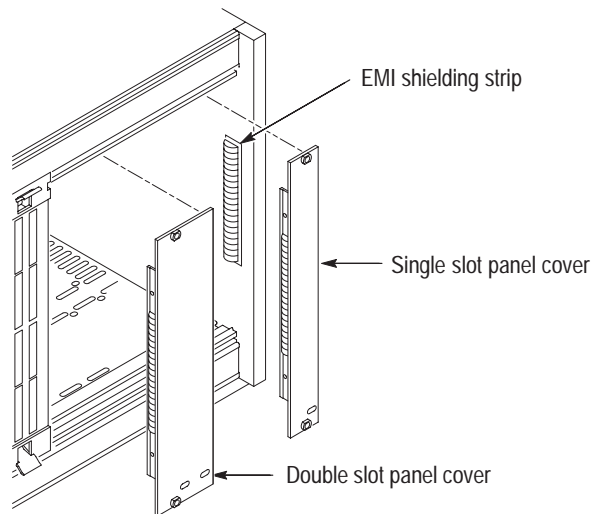


Figure D-5: Installing panel covers on the benchtop mainframes

Appendix E: Merging Modules

This appendix describes how to merge TLA700 series logic analyzer and pattern generator modules to form wider modules.

A merged logic analyzer module set consists of a master logic analyzer module and one or two slave logic analyzer modules physically connected together by a merge cable, and merged in software. Review the guidelines under *Logic Analyzer Module Merging Rules* and then follow the steps to physically connect the modules together before installing the modules in the mainframe.

A merged pattern generator module set consists of a master pattern generator module and up to four slave pattern generator modules merged in software. Review the guidelines under *Pattern Generator Module Merging Rules* on page E-3 before installing the modules in the mainframe.

Logic Analyzer Module Merging Rules

The following logic analyzer module merging rules must be followed:

- Only modules with 102 channels or more can be merged.
- Logic analyzer modules must be in adjacent slots and physically connected.
- Logic analyzer modules can not be merged across mainframes (between the benchtop mainframe and one or more expansion mainframes), because the modules must be physically adjacent and physically connected.
- Logic analyzer modules of unequal synchronous clock rate can not be merged.
- Merging logic analyzer modules of unequal memory depths will result in the merged modules assuming the depth of the shallowest module.
- When merging logic analyzer modules of unequal channel widths, use the logic analyzer module with the higher number of channels as the master module.
- The logic analyzer modules must have the same firmware version.
- Two or three TLA7Nx, TLA7Px, or TLA7Qx logic analyzer modules can be merged together. Two TLA7Lx and TLA7Mx logic analyzer modules can be merged together.
- TLA7Nx, TLA7Px, and TLA7Qx Logic analyzer modules can not be merged with TLA7Lx and TLA7Mx Logic analyzer modules. (Even if they are connected together.)

- Merging operations may not be destructive to an established merged logic analyzer module set. To merge a logic analyzer module to an established merged set, the established merged set must first be unmerged through software. Unmerged modules are the only potential candidates to add to a merged configuration.

Two Way Logic Analyzer Merge

In a two way merge, the master module is on the left (lower-numbered slot) and the slave module is on the right as shown in Figure E-1.

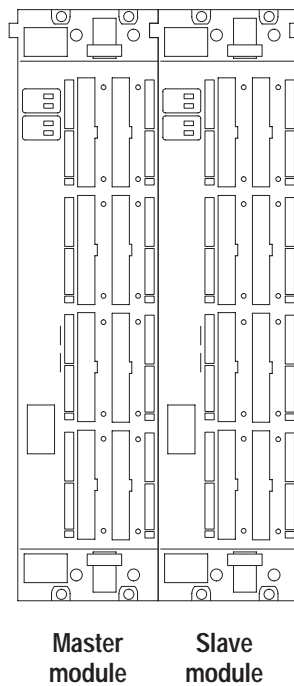


Figure E-1: Location of modules in a two way merge

Three Logic Analyzer Way Merge

In a three way merge (TLA7Nx, TLA7Px, or TLA7Qx logic analyzer modules only), the master module is in the center. Slave module 1 is to the right of the master module. Slave module 2 is on the left of the master module as shown in Figure E-2.

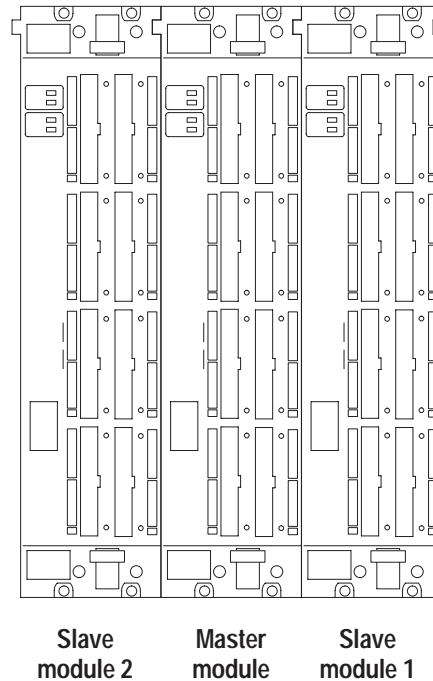


Figure E-2: Location of modules in a three way merge

Pattern Generator Module Merging Rules

The following pattern generator module merging rules must be followed:

- Pattern generator modules are merged through software.
- Pattern generator modules must be physically adjacent.
- Pattern generator modules may not be merged across mainframes.
- Merging pattern generator modules of unequal memory depths will result in the merged set assuming the depth of the shallowest pattern generator module.
- Pattern generator modules must have the same firmware version.
- When merged, the left-most pattern generator module is the master.

Logic Analyzer Merge Procedures

Use the following procedures to physically merge the logic analyzer modules together.

Two Way Logic Analyzer Merge Procedure

The following procedure is used for merging two logic analyzer modules to form a merged set with a higher logic analyzer channel count. For information on merging three modules, see page E-9.



CAUTION. *Static discharge can damage any semiconductor component in the logic analyzer module.*

Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while performing the merge procedure.

Perform the following steps to merge two modules:

1. Turn the mainframe off.
2. Determine which module will be designated as the slave module and which module will be the master module.
3. Lay the slave module on the right side (as viewed from the front panel).
4. Remove the screws from the module cover with a screwdriver with a T-10 Torx tip; refer to Figure E-3 on page E-5.
5. Remove the screws near the front of the module.
6. Remove the screws holding the merge cable bracket to the cover.
7. Remove the top part of the cable bracket and set it aside.
8. Remove the module cover and locate the merge cable.

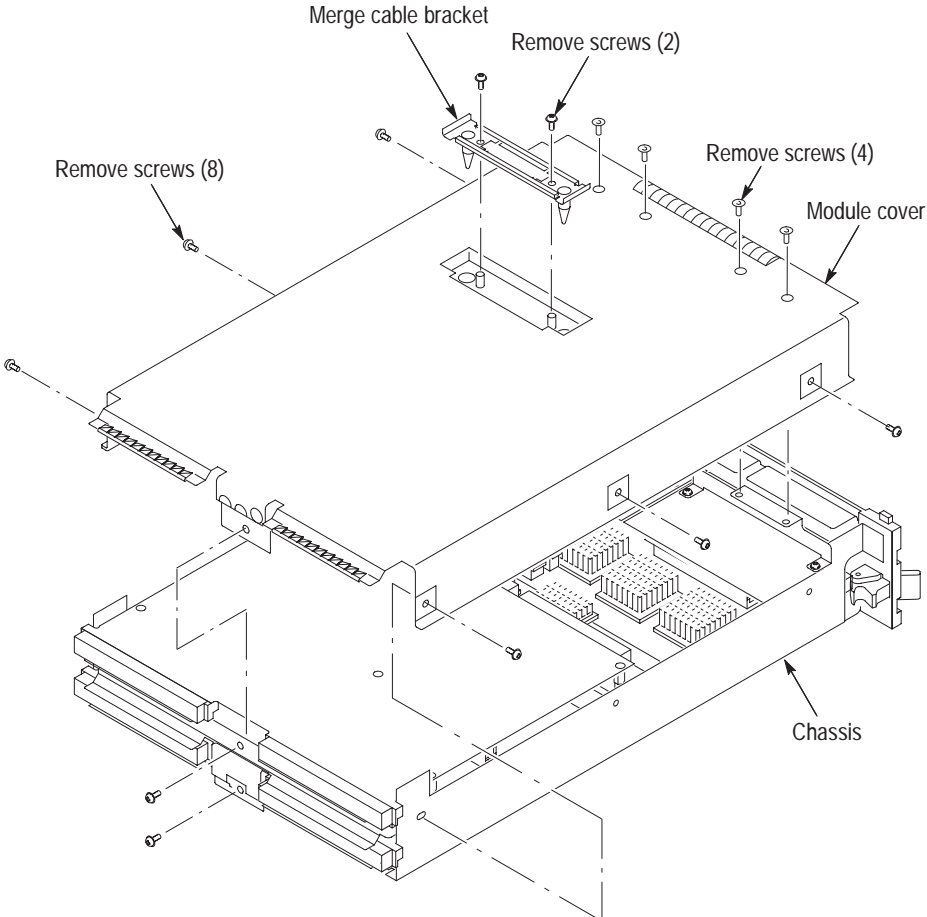


Figure E-3: Removing the cover

9. Replace the cover while feeding the merge cable through the hole in the cover (see Figure E-4).

Do not twist the cable while feeding it through the hole. If the cable is twisted, the modules will not mate correctly.

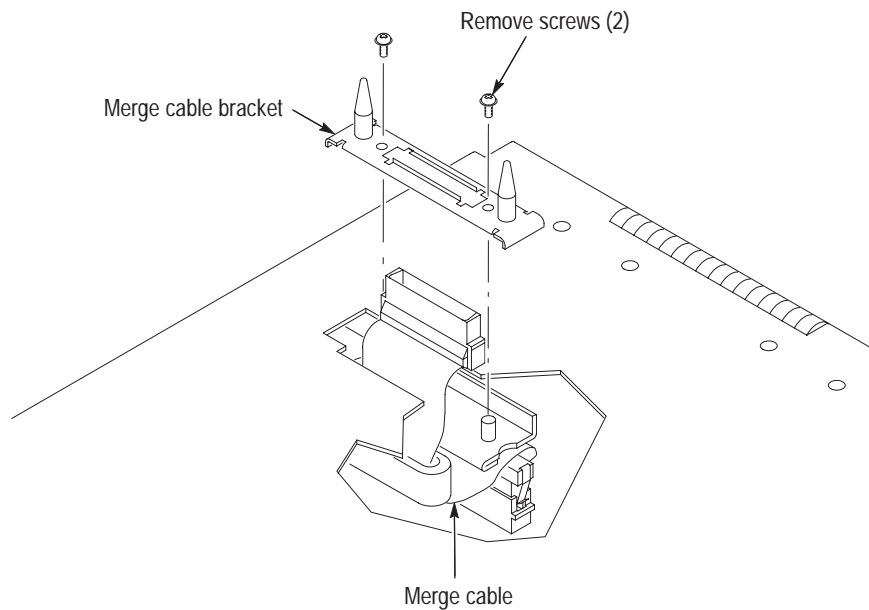


Figure E-4: Feeding the merge cable through the cover

10. Turn the merge cable bracket over so that the guide pins point up.
11. Place the bracket over the merge cable connector.
12. Install the two screws that hold the merge cable bracket in place.



CAUTION. To prevent damage to the module during the installation process, reinstall the cover exactly as described in steps 14 through 19.

If the cover is not properly seated, the module can be damaged when you install it in the mainframe and it will not meet EMC requirements.

13. Replace the logic analyzer module cover.
14. Push forward on the cover so the tab on the front edge of the cover inserts into the rear of the front subpanel. Make sure that the cover is fully seated (no gaps) against the front and rear chassis flanges.

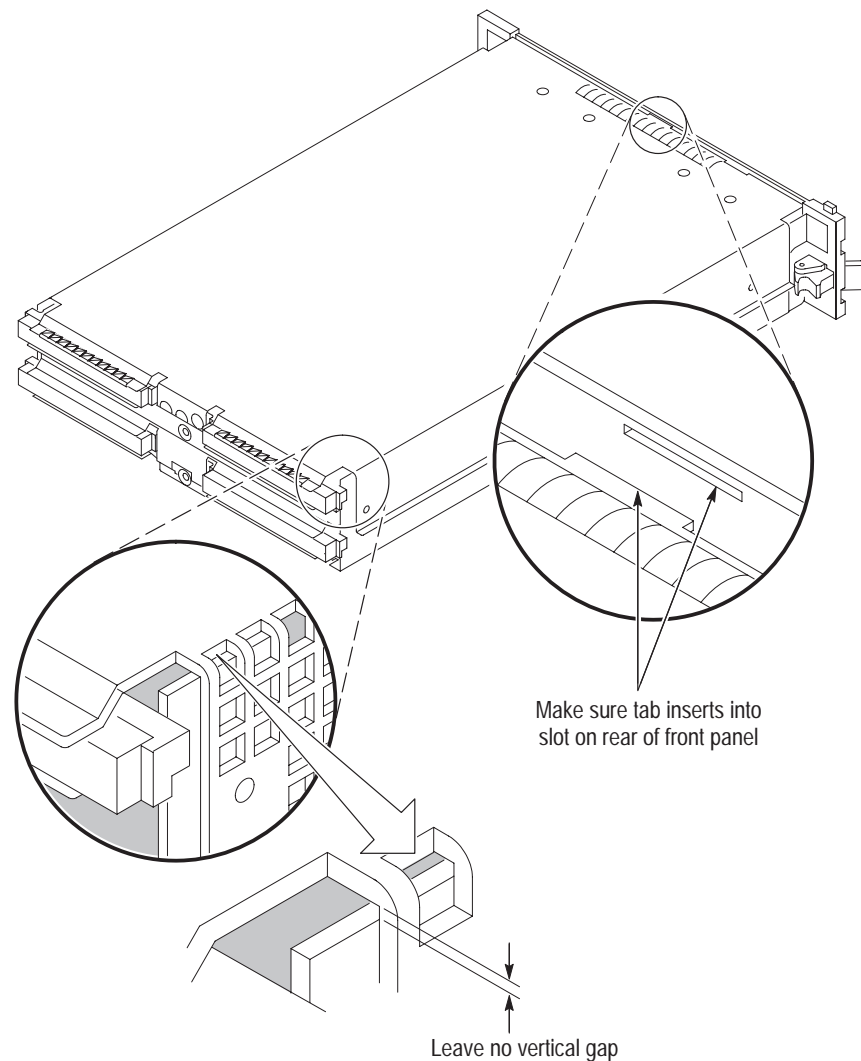


Figure E-5: Seating the cover on the chassis

15. While holding the cover in place, install the screws nearest the front of the module (two on the top and two on the bottom), to secure the cover to the chassis.
16. Install the screws near the front of the module.
17. Slide the rear panel on the chassis and install the rear panel screws.

18. Install the top and bottom rear screws.
19. Check and tighten all screws.
20. Place the master module adjacent to the slave module so that the two guide pins from the Slave module line up with the guide pin holes in the master module.

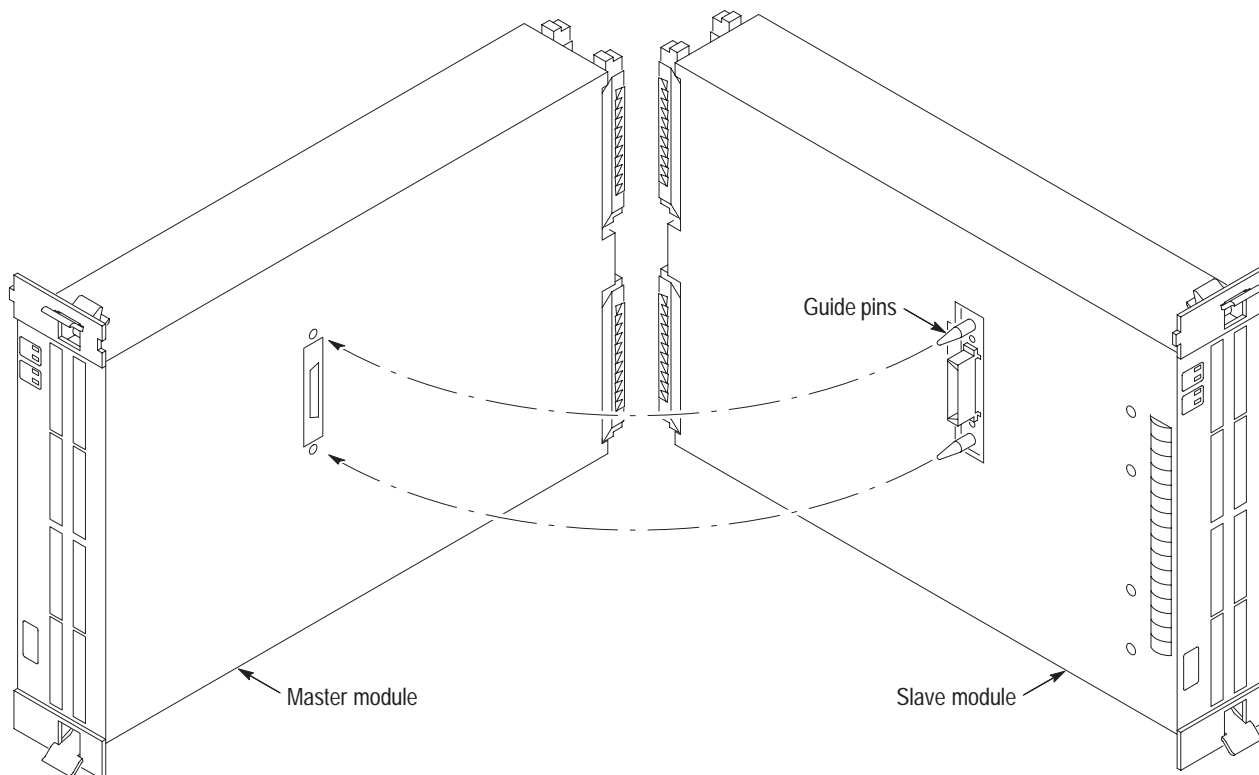


Figure E-6: Lining up the two modules

21. Gently push the two modules together so that the merge connector of the slave module mates with the merge connector on the master module.

Three Way Logic Analyzer Merge Procedure

The following procedure is used for merging three logic analyzer modules together to form a merged set with a higher logic analyzer channel count.

In a three way merge (TLA7Nx, TLA7Px, and TLA7Qx logic analyzer modules only), the master module is in the center. Slave module 1 is to the right of the master module. Slave module 2 is on the left of the master module as shown in Figure E-2 on page E-3.



CAUTION. *Static discharge can damage any semiconductor component in the logic analyzer module.*

Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while performing the merge procedure.

Perform the *Two Way Logic Analyzer Merge Procedure* beginning on page E-4.

Perform the following steps to merge the second slave module:

1. Lay the two merged module set on their right hand side (as viewed from the front panel).
2. Follow the procedure beginning on page E-4 to merge the second slave module to the left of the center master module.

Installing the Merged Logic Analyzer Modules in the Mainframe

After merging the modules, perform the following steps to install the merged modules in the mainframe:

1. Hold the merged modules such that the modules do not become separated and line up the modules with the slot guides in the mainframe.
2. Push the merged modules into the mainframe until they rest against the rear panel connector.
3. Use the injector/ejector handles to fully seat the modules one at a time. Tighten the module retainer screws.
4. Verify that the modules are fully seated before powering on the mainframe.

Calibrating the Merged Modules

Always calibrate each module separately, then calibrate the merged set.

After powering on the mainframe, calibrate the merged modules by following these steps:

1. Select the System window. If you are calibrating pattern generator modules, select the System window from the pattern generator application.
2. From the menu bar, select System.
3. Select Calibration and Diagnostics.
4. Select the Self Calibration tab.
5. Select (highlight) the modules to be calibrated.
6. Press the Run button in the merge calibrate dialog box.

Removing Merged Logic Analyzer Modules from the Mainframe

Perform the following steps to remove merged modules from the mainframe:

1. Identify the modules that you want to remove.
2. Loosen the retainer screws for the modules (top and bottom).

NOTE. Use the ejector handles to just loosen the modules from the rear panel connector before sliding the merged modules out of the mainframe.

3. Use the ejector handles to disconnect the modules from the rear panel connector one at a time.
4. Slide the modules out of the mainframe at the same time.
5. Gently pry the modules apart.

Storing the Logic Analyzer Module Merge Cable

Perform the following steps to store the logic analyzer merge cable inside the logic analyzer module:

1. Use the screwdriver with the T-10 Torx tip to remove the screws that hold the merge cable bracket in place.
2. Remove the merge cable bracket.
3. Remove the screws from the side cover and rear cover.
4. Push the merge cable through the side cover and remove the cover.
5. Dress the merge cable as shown in Figure E-7.

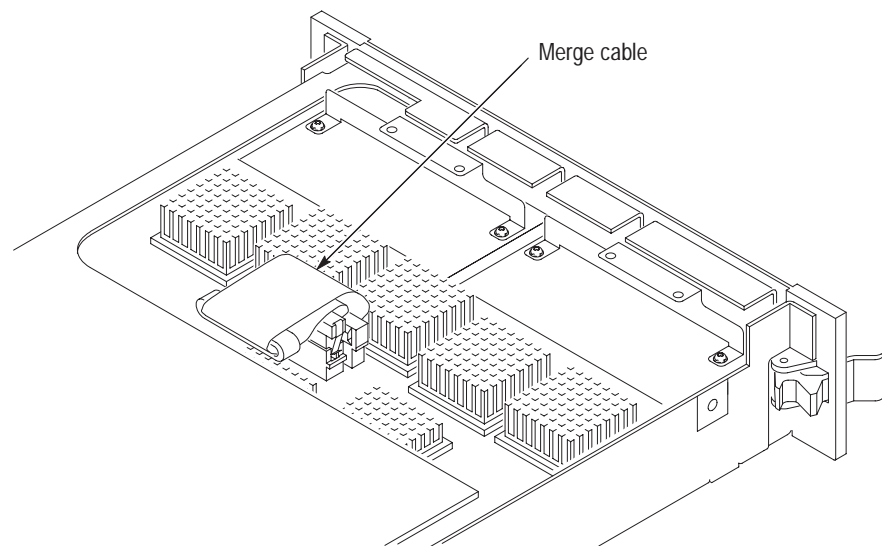


Figure E-7: Dressing the merge cable before installing the cover

6. Push forward on the cover so the tab on the front edge of the cover inserts into the rear of the front subpanel. Make sure that the cover is fully seated and there are no gaps between the front and rear chassis flanges; refer to Figure E-5.
7. While holding the cover in place, install the screws nearest the front of the module to secure the cover to the chassis.
8. Install the screws near the front of the module.
9. Slide the rear panel on the chassis and install the rear panel screws.

- 10.** Install the top and bottom rear screws.
- 11.** Install the merge cable bracket so that the guide pins point into the module.
- 12.** Install and tighten the screws on the merge cable bracket.
- 13.** Verify that you have installed and tightened all screws on the module.

Appendix F: Power Cord and Line Fuse Requirements for the Benchtop and Expansion Mainframes

The benchtop and expansion mainframes come with two power cords and three fuses (one fuse is already installed).

You must determine the correct fuse and power cord for your configuration. This is important to avoid overloading the power distribution system and ensures that you comply with the National Electrical Code.

The power consumption depends on the number and type of instrument modules installed in the mainframes. Table F-1 lists the power consumed for each module.

To determine the total power consumption, perform the following steps:

1. Use Table F-1 to determine the power consumption for each module.
2. Add the power for each module to determine the total power consumption.
3. Determine at which line voltage you will be operating.
4. Refer to Figure F-1 on page F-2 to determine the proper power cord and line fuse for your mainframe.

Table F-1: Power for instrument modules

Module type	Power (Watts)
TLA720 Benchtop Controller	50
TLA7XM Expansion Module	20
TLA7Q2	82
TLA7Q4	108
TLA7P2	82
TLA7P4	108
TLA7N1	70
TLA7N2	82
TLA7N3	74
TLA7N4	108
TLA7L1	55
TLA7L2	73
TLA7L3	94
TLA7L4	109

Table F-1: Power for instrument modules (Cont.)

Module type	Power (Watts)
TLA7M1	57
TLA7M2	76
TLA7M3	99
TLA7M4	115
TLA7D1	56
TLA7D2	81
TLA7E1	56
TLA7E2	81

For power usage in the unshaded region of Figure F-1, use either the power cord with the 15 A plug (two parallel prongs and ground) or the power cord with the 20 A plug (two perpendicular prongs and ground).

For high power usage combined with low input line voltages (shaded region), use only the power cord with the 20 A plug. Select the proper fuse based on the ranges shown in Figure F-1.

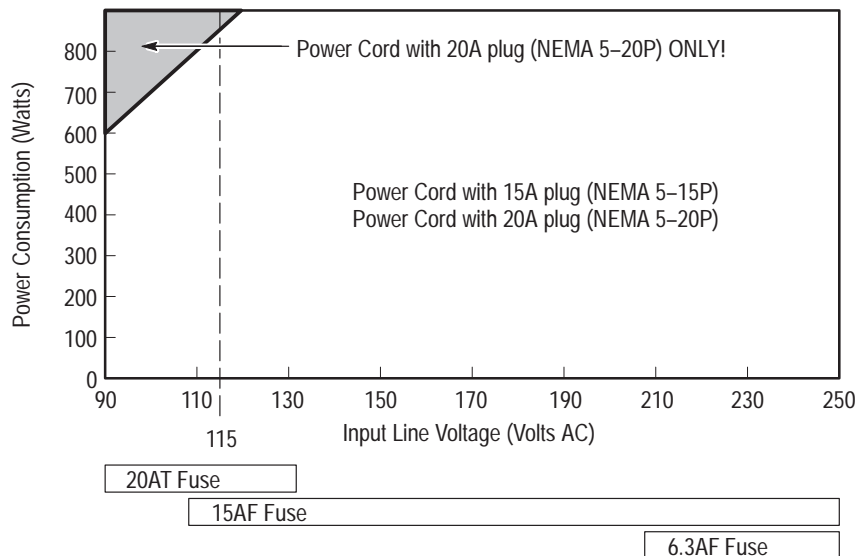


Figure F-1: Power cord identification chart

For example, assume that your configuration consists of four TLA7M4 Logic Analyzer Modules and one TLA7E2 DSO Module. Also assume that you will be operating the mainframe at 90 VAC.

Add 50 Watts (for the benchtop controller) + 81 Watts (for the DSO Module) + 4 X 115 Watts (for the logic analyzer modules) to come up with a total value of 591 Watts.

Because the power consumption (at 90 VAC) is approaching the shaded area of the graph in Figure F-1, you should consider using the 20A power cord.

NOTE. *If you are configuring an expansion mainframe, remember to use the power value for the expansion module instead of the benchtop controller.*

Appendix G: Installing Software

This section describes procedures for reinstalling software or firmware on the Tektronix logic analyzer. Most of the software comes factory-installed when you receive your logic analyzer. Refer to this appendix when you need to reinstall your software.



CAUTION. *The software installation procedure will overwrite the **entire contents** of your hard disk. If you want to save any files or software applications on the hard disk, back them up to another media (a second hard drive, floppy disks, or a network drive) before continuing with this procedure.*

Installing Software

This section provides information for installing software in your logic analyzer. In addition to the Tektronix Logic Analyzer application software, there are other software programs that are installed separately; Table G–1 lists some of the software that you may have installed on your logic analyzer.

Table G–1: Software not covered by the software setup

Software	Installation information
Microprocessor or bus support software	Refer to the manual that was shipped with the microprocessor or bus support.
PC Card Software	Refer to the instructions that come with your PC Card.
Other Software	Refer to the instructions that come with your software.

Flashing the BIOS

You may need to flash the controller BIOS on your logic analyzer to update the controller with the latest flash image before reinstalling software on the hard disk. The procedures for flashing the BIOS differ between the TLA600 logic analyzers and the TLA700 logic analyzers. Refer to the proper procedure before flashing the BIOS image on your logic analyzer.

Flashing the BIOS on the TLA600 Logic Analyzer

This procedure is only necessary if you need to update the latest flash image. To flash the BIOS, complete the following steps:

1. Exit all applications and power off the logic analyzer.
2. Insert the TLA600 BIOS disk, Version P09, in the floppy disk drive.
3. Power on the logic analyzer and allow the logic analyzer to boot from the floppy disk. After booting from the floppy disk, the program on the floppy disk will automatically flash the BIOS on the TLA600 controller.
4. Wait for the flash procedure to complete.
5. After the flash procedure has completed, power off the logic analyzer and remove the floppy disk.



CAUTION. Do not remove the floppy disk drive or power down the logic analyzer during the flash operation. Doing so will cause the system to become inoperable.

Setting Up the TLA600 Controller BIOS

This procedure is necessary after replacing the hard disk or when the CMOS settings are corrupted or lost. To configure the Controller BIOS, complete the following steps:

1. Power on the logic analyzer and press function key F2 before the logic analyzer boots the Windows operating system.
2. Press function key F9, select Yes, and then press Enter to set the default settings. Verify that the hard disk was auto-recognized and that the correct size of the hard disk is displayed in the Primary Master setting.
3. Verify that all of the settings are the same as the settings in Table G-2.
4. Press function key F10 to exit and save the BIOS setup.

Table G-2: TLA600 Controller BIOS setup

Parameter	Setting/Description	2 nd Field setting	Memo
Main			
Processor Type	Intel Celeron		No active selections
Processor Speed	500 MHz		No active selections
Cache RAM	128 KB		No active selections
Total Memory	64 MB		64 MB or 128 MB
Memory Bank 0	64 MB		
Memory Bank 1	Not Installed		Will be installed as an option
System Time	<i>Set to current time</i>		
System Date	<i>Set to current date</i>		
Advanced			
▶ Boot Configuration			
Plug & Play O/S	[No]		
Reset Configuration Data	[No]		
Numlock	[Off]		
▶ Peripheral Configuration			
Serial Port A	[Auto]		
Serial Port B	[Disabled]		
Parallel Port	[Auto]		
Mode	[ECP]		
Audio Device	[Enabled]		
LAN Device	[Enabled]		
Legacy USB Port	[Enabled]		
▶ IDE Configuration			
IDE Controller	[Both]		
Hard Disk Pre-Delay	[Disabled]		
▶ Primary IDE Master	[Mfg. name – model] (HDD)		e.g.: Autodectable
▶ Primary IDE Slave	[Not installed]		
▶ Secondary IDE Master	[Mfg. name – model] (CD ROM)		e.g.: Autodectable
▶ Secondary IDE Slave	[Not installed]		

Table G-2: TLA600 Controller BIOS setup (Cont.)

Parameter	Setting/Description	2 nd Field setting	Memo
▶ Diskette Configuration			
Diskette Controller	[Enabled]		
Floppy A	[1.44/1.25 MB 3 1/2]		
Diskette Write Protect	[Disabled]		
▶ Event Log Configuration			
Event Log	[Space Available]		Not Active Selections
Event Log Validity	[Valid]		Not Active Selections
▶ View Event Log		Event Log: Pre-Boot Error: CMOS Checksum Error	On the 2 nd attempt reading "No unread events"
Clear Event Log	[No]		
Event Logging	[Enabled]		
▶ Mark Events as Read		[Yes]	
▶ Video Configuration			
Primary Video Adapter	[PCI]		PCI = Internal Display AGP = External Monitor
▶ Security			
Supervisor Password Is	[Not Installed]		Not Active Selections
User Password Is	[Not Installed]		Not Active Selections
▶ Set Supervisor Password		Enter Password	
▶ Set User Password		Enter Password	
▶ Power			
Power Management	[Enabled]		
Inactivity Timer	[Off]		
Hard Drive	[Enabled]		
Video Power Down	[Disabled]		
ACPI Suspend State	[S1 State]		
▶ Boot			
Quiet Boot	[Disabled]		
Quick Boot	[Enabled]		
Scan Upper Flash Area	[Disabled]		
After Power Failure	[Last State]		
On Modem Ring	[Stay Off]		
On LAN	[Power On]		

Table G-2: TLA600 Controller BIOS setup (Cont.)

Parameter	Setting/Description	2 nd Field setting	Memo
On PME	[Stay Off]		
1 st Boot Device	[Floppy]		
2 ^{ed} Boot Device	[IDE-HDD]		
3 ^{ed} Boot Device	[ATAPI CDROM]		
4 th Boot Device	[Intel UNDI, PXE-2.0 (b)]		
5 th Boot Device	[Disabled]		
▶ IDE Drive Configuration			
	▶ Primary IDE Master	[1 st IDE]	
	▶ Primary IDE Slave	[2 nd IDE]	
	▶ Secondary IDE Master	[3 rd IDE]	
	▶ Secondary IDE Slave	[4 th IDE]	
▶ Exit			
▶ Exit Saving Changes	Yes or No		
▶ Exit Discarding Changes	Yes or No		
▶ Load Setup Defaults	Yes or No		
▶ Load Custom Defaults	Yes or No		
▶ Save Custom Defaults	Yes or No		
▶ Discard Changes	Yes or No		

Flashing the BIOS on the TLA700 Logic Analyzers

This procedure is only necessary if you need to update the latest flash image. To flash the BIOS, complete the following steps:

1. Power on the logic analyzer and press function key F2 before the Windows operating system starts. The BIOS Setup menu displays.
2. From the BIOS Setup menu, go to the Exit menu.
3. Insert the TLA700 BIOS disk in the floppy disk drive.
4. From the Exit menu, choose Exit & Update BIOS.
5. When the system displays a dialog box asking if you want to proceed with the Flash update, confirm your choice.

The display goes blank during the flash operation, which lasts about one minute. When the BIOS update is complete, the logic analyzer automatically reboots.

6. Remove the BIOS disk from the floppy disk drive.



CAUTION. Do not remove the floppy disk drive or power down the logic analyzer during the flash operation. Doing so will cause the system to become inoperable.

Setting Up the TLA700 Controller BIOS

This procedure is necessary after replacing the hard disk or when the CMOS settings are corrupted or lost. To configure the Controller BIOS, complete the following steps:

1. Power on the logic analyzer and press function key F2 before the logic analyzer boots the Windows operating system.
2. Press function key F9, select Yes and then press Enter to set the default settings. Verify that the hard disk was auto-recognized and that the correct size of the hard disk is displayed in the Primary Master setting.
3. Verify that all of the settings are the same as the settings in Table G-3.
4. Press function key F10 to exit and save the BIOS setup.

Table G-3: TLA714 and TLA720 Controller BIOS setup

Parameter	Factory setting	Submenu parameter	Factory setting
Main			
System Time	<i>Set to current time</i>		
System Date	<i>Set to current date</i>		
Legacy Diskette A	[1.44/1.25 MB, 3 1/2"]		
▶ Primary Master	<i>hard disk drive size</i>		
		Type	[Auto]
		Cylinders	<i>Set by Autotype</i>
		Heads	<i>Set by Autotype</i>
		Sectors	<i>Set by Autotype</i>
		Maximum Capacity	<i>Set by Autotype</i>
		Multi-sector transfers	<i>Set by Autotype</i>
		LBA Mode Control	<i>Set by Autotype</i>
		32-Bit I/O	[Disabled]
		Transfer Mode	<i>Set by Autotype</i>
		Ultra DMA Mode	<i>Set by Autotype</i>
▶ Primary Slave	[None]		
▶ Secondary Master	[CD-ROM]		
▶ Secondary Slave	[None]		
Enable SimlScan	[Disabled]		
Summary Screen	[Disabled]		
▶ Memory Cache			
		Memory Cache	[Enabled]
		External Cache	[Disabled]
		Cache System BIOS area:	[Enabled]
		Cache Video BIOS area:	[Disabled]
		Cache D000 – D3FF:	[Disabled]
		Cache D400 – D7FF:	[Disabled]
		Cache D800 – DBFF:	[Disabled]
System Memory	640 KB		
Extended Memory	<i>Installed memory – 640 K</i>		

Table G-3: TLA714 and TLA720 Controller BIOS setup (Cont.)

Parameter	Factory setting	Submenu parameter	Factory setting
Advanced			
▶ I/O Device Configuration			
		Local Bus IDE Adapter	[Both]
		Serial port A	[Enabled]
		Base I/O Address	[3F8]
		Interrupt	[IRQ4]
		Serial port B	[Enabled]
		Mode	[Normal]
		Base I/O Address	[2F8]
		Interrupt	[IRQ3]
		Parallel Port	[Enabled]
		Mode	[ECP]
		Base I/O Address	[378]
		Interrupt	[IRQ7]
		DMA Channel	[DMA 1]
		Floppy disk controller	[Enabled]
▶ Advanced Chipset Control			
		DRAM Speed	[60 ns]
		DMA Aliasing	[Enabled]
		16 Bit I/O Recovery	[4.5]
		8 Bit I/O Recovery	[4.5]
Plug & Play O/S	[Yes]		
Reset Configuration Data	[No]		
PS/2 Mouse	[AutoDetect]		
Large Disk Access Mode:	[Other]		
Secured Setup Configurations	[No]		
▶ PCI Configuration			
		ISA graphics device installed	[No]
		▶ PCI/PNP ISA UMB Region Exclusion	
		C800 – CBFF	[Available]
		CC00 – CFFF	[Available]
		D000 – D3FF	[Available]

Table G-3: TLA714 and TLA720 Controller BIOS setup (Cont.)

Parameter	Factory setting	Submenu parameter	Factory setting
		D400 – D7FF	[Available]
		D800 – DBFF	[Available]
		DC00 – DFFF	[Available]
		▶ PCI/PNP ISA IRQ Resource Exclusion	
		IRQ3	[Available]
		IRQ4	[Available]
		IRQ5	[Available]
		IRQ7	[Available]
		IRQ9	[Available]
		IRQ10	[Available]
		IRQ11	[Available]
		IRQ14	[Available]
		IRQ15	[Available]
Power			
Power Savings	[Disabled]		
Standby Timeout:	[Off]		
Auto Suspend Timeout	[Off]		
Resume On Time	[Off]		
IDE Drive 0 Monitoring	[Disabled]		
IDE Drive 1 Monitoring	[Disabled]		
IDE Drive 2 Monitoring	[Disabled]		
IDE Drive 3 Monitoring	[Disabled]		
PCI Bus Monitoring	[Disabled]		

Table G-3: TLA714 and TLA720 Controller BIOS setup (Cont.)

Parameter	Factory setting	Submenu parameter	Factory setting
Boot			
1.	[Diskette Drive]		
2.	[Removable Devices]		
3.	[Hard Drive]		
4.	[ATAPI CD-ROM Drive]		
▶ Hard Drive			
		1.	<i>Currently installed drive ID</i>
		2.	[Bootable Add-in Card]
▶ Removable Devices			
Exit			
▶ CMOS Save & Restore			
		CMOS Restore Condition	[Never]

Reinstalling the Hard Disk Image

The Tektronix Logic Analyzer comes with a CD containing Microsoft Windows 2000 Professional operating system and the latest application software. All software required to run the logic analyzer comes with the CD with the exception of any Microprocessor support packages or non-logic analyzer application software. The process of reloading the software on the hard disk will destroy any files or programs installed on the hard disk.

Use the appropriate CD for your application. For TLA700 instruments, use the CD entitled *TLA700 Hard Disk Image*. For TLA600 instruments, use the CD entitled *TLA600 Hard Disk Image*.



CAUTION. *The software installation procedure will destroy the **entire contents** of your hard disk. If you want to save any files or software applications on the hard disk, back them up to another media (a second hard drive, floppy disks, or a network drive) before continuing with this procedure.*

Backing Up Files

Before loading the Hard Disk Image software, make sure that you back up any files, applications, and personal documents to an external storage device. You can do this in one of several different ways:

- Move the files to another PC via a network or via another backup medium such as a ZIP drive.
- If you have a TLA700 series logic analyzer, purchase the TLA7UP Option 10, place the new hard disk drive in the removeable hard disk drive assembly, and then place the original hard disk drive in the second hard disk location. This allows you to use a second hard disk drive so you can still access the user files. You may need to refer to the service documentation for information on installing a second hard disk.

You can find most TLA user files using the Windows Find utility. For example, open Windows Explorer and select the C:\My Documents folder. Right click on the folder and select Find. Enter one of the suffixes from Table G-4 to locate the files in the current folder and all subfolders:

Table G-4: TLA user file suffixes

Suffix	Description
.tla	TLA setup files
.tsf	TLA symbol files
.tbf	Tektronix binary format
.tls	TLA script file

Once you find the files, copy or drag them to the external storage device. Use this procedure to find any files or applications that you may want to save.

If you purchased any microprocessor support packages, you will need to reinstall the application after you reinstall the hard disk image. If you don't have a copy of the microprocessor support software, contract your Tektronix Account Manager to order a replacement copy. If you cannot contact the account manager, contact the Tektronix Support Center (refer to *Contacting Tektronix* on page xix at the beginning of this document).

Installing Windows 2000 Professional and the TLA Application Software

This procedure automatically reformats the hard disk, installs the Windows 2000 Professional Operating system software, and installs the the Tektronix Logic Analyzer application software. Because this procedure reformats the hard disk drive, be sure to back up any files or software that you want to preserve by following the steps in the previous section.

NOTE. *After installing the hard disk image, you must reset the BIOS boot settings to the Tektronix defaults.*

Change the BIOS Boot Settings. Before installing the Hard Disk Image, you must change the BIOS settings.

1. Restart the logic analyzer and then press function key F2 to enter the BIOS setup.
2. In the BIOS setup, go to the Boot menu.
3. Set the Boot devices as shown below (items in parenthesis refer to TLA600 settings):

First Boot Device:	[ATAPI CDROM Drive]
Second Boot Device:	[Diskette Drive] (Floppy)
Third Boot Device:	[Hard Drive] (IDE-HDD)

4. Save the settings by pressing function key F10 and confirm that you want to save the new settings.

Load the Hard Disk Image. Complete the following steps to load the Hard Disk Image.

1. Insert the Hard Disk Image CD in the CDROM drive.
2. Reboot the logic analyzer.
3. Review the license agreement. If you agree to the terms of the license agreement, proceed with the next step.

NOTE. *Use care when prompting through the software license agreement to avoid confirming that you want to cancel the software installation procedure.*

4. When you have completed reviewing the software license agreement, the EasyRestore dialog box displays and prompts you to either continue or cancel the upgrade process. Click Continue to begin loading the contents of the upgrade CD.
5. The EasyRestore program displays a warning that the contents of your hard disk will be destroyed if you choose to continue. Click Yes to continue the process.
6. The program will automatically start and guide you through the rest of the procedure. The image loading procedure is fully automatic and takes approximately 15 minutes to complete.

The image loading procedure automatically installs and sets up the logic analyzer application. You should not need to make any changes to the setup to use the logic analyzer.

7. After the image is loaded, remove the CD from the CDROM drive and reboot the logic analyzer.
8. The Systems Settings Change error message displays, prompting you to restart the instrument before your changes can take effect. Click Yes to restart the instrument.
9. Reinstall any user files that you backed up previously. Reinstall any software (such as the microprocessor support packages) that you want to use on the logic analyzer.
10. If desired, reconfigure the TLA network interface.

Reset the BIOS Boot Settings. After you have successfully installed the hard disk image, you should reset the BIOS boot settings so that your logic analyzer boots properly.

1. Restart the logic analyzer and then press function key F2 to enter the BIOS setup.
2. In the BIOS setup, go to the Boot menu.
3. Set the Boot devices as shown below (items in parenthesis refer to TLA600 settings):

First Boot Device:	[Diskette Drive] (Floppy)
Second Boot Device:	[Removable Devices]
Third Boot Device:	[Hard Drive] (IDE-HDD)
Fourth Boot Device:	[ATAPI CDROM Drive]

4. Save the settings by pressing function key F10 and confirm that you want to save the new settings.

Updating TLA700 Module Firmware

Perform the following steps if you need to reinstall or update the flash ROM-based firmware on your modules. You can update multiple modules and module types during a single firmware update session.

1. Turn off the logic analyzer.
2. Disconnect the power cord.
3. Disconnect any probes on the modules that you want to upgrade.
4. Remove the module from the logic analyzer.
5. Refer to Figure G–1 and locate the flash programming pins on the rear of the module.
6. Install a jumper on the flash programming pins (use one of the spare jumpers that came with your logic analyzer).
7. Reinstall the module(s) in the logic analyzer.
8. Reconnect the power cord and turn on the logic analyzer.

NOTE. Any modules with the flash programming jumper installed will not display in the System window.

9. Exit the logic analyzer application.
10. Click Start, point to Programs, point to Tektronix Logic Analyzer, and click TLA Firmware Loader.
11. Select the modules that you want to update from the list of modules displayed in the Supported list box near the top of the menu. If you are updating more than one module at a time, note the slot location of the module in the selection box.

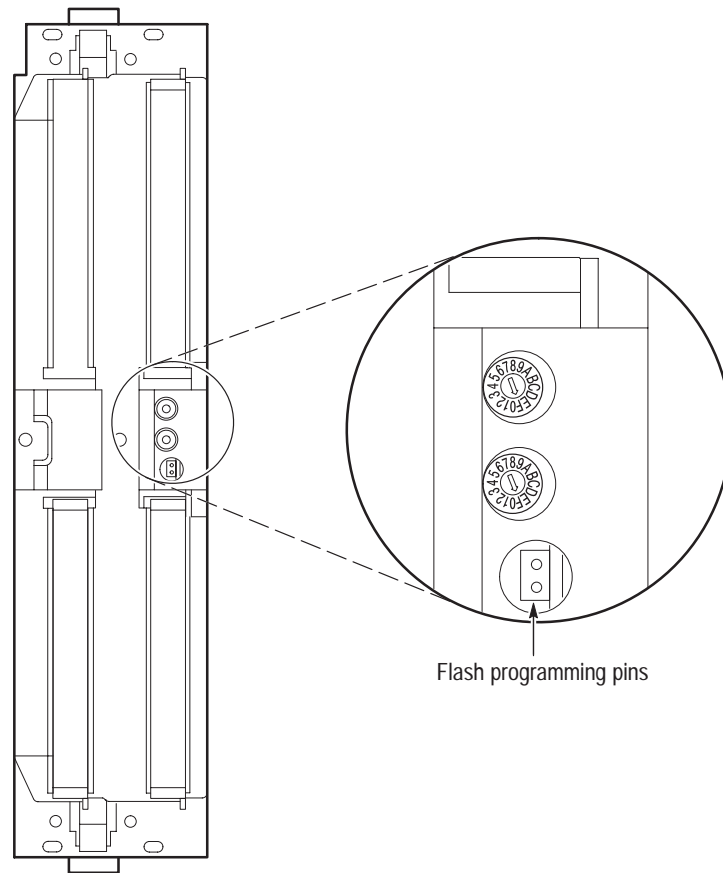


Figure G-1: Flash programming pins

12. Select Load Firmware from the Execute menu.

13. Click the proper .LOD file for the module in the:

C:\Program Files\TLA700 Firmware directory, or the

C:\Program Files\Tektronix Pattern Generator Firmware directory.

If you are updating more than one module make sure that you select the proper firmware file for the module in the listed slot number.

14. Click OK. You will be asked to confirm your action; click Yes when prompted.

NOTE. The program will not allow you to load firmware to an incompatible module. For example, the program will not load DSO firmware to a logic analyzer module.

15. If you are updating another module, select the proper .LOD file for the module.

16. Click OK. You will be asked to confirm your action; click Yes when prompted.

The program will load the firmware for each module one at a time. The process takes approximately five minutes per module.

17. Exit the program.

18. Turn off the logic analyzer and disconnect the power cord.

19. Remove the module from the logic analyzer and remove the jumper from the Flash programming pins on the rear of the module. Keep the jumper for future updates.

20. Attach a new label with the new firmware version to the module.

21. Reinstall the module in the logic analyzer and reconnect the probes.

22. Reconnect the power cord and turn on the logic analyzer.

23. Verify that the power-on diagnostics pass.

24. Run the self calibration on each module after a 30-minute warm-up.

Appendix H: User Service

This appendix describes service information and procedures for the Tektronix logic analyzers. Mainframe and module service troubleshooting procedures are located in the service manuals.

Service Offerings

Tektronix provides service to cover repair under warranty as well as other services that are designed to meet your specific service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians are well equipped to service the logic analyzers. *Services are provided at Tektronix Services Centers and on-site at your facility, depending on your location.*

Warranty Repair Service

Tektronix warrants this product for one year from date of purchase. (The warranty appears behind the title page in this manual.) Tektronix technicians provide warranty service at most Tektronix service locations worldwide. The Tektronix product catalog lists all service locations worldwide or you can visit us on our *Customer Services World Center* web site at:

www.tektronix.com/Measurement/Service

Calibration and Repair Service

In addition to warranty repair, Tektronix Service offers calibration and other services which provide cost-effective solutions to your service needs and quality-standards compliance requirements. Our instruments are supported worldwide by the leading-edge design, manufacturing, and service resources of Tektronix to provide the best possible service.

The following services can be tailored to fit your requirements for calibration and/or repair of the TLA logic analyzers:

Service Options. Tektronix Service Options can be selected at the time you purchase your instrument. You select these options to provide the services that best meet your service needs. These service options are listed on the *Tektronix Service Options* page following the title page of this manual.

Service Agreements. If service options are not added to the instrument purchase, then service agreements are available on an annual basis to provide calibration services or post-warranty repair coverage for the TLA logic analyzers. Service agreements may be customized to meet special turn-around time and/or on-site requirements.

Service on Demand. Tektronix also offers calibration and repair services on a “per-incident” basis that is available with standard prices for many products.

Self Service. Tektronix supports repair to the replaceable-part level by providing for circuit board (module) exchange.

Use this service to reduce down-time for repair by exchanging faulty circuit boards for remanufactured ones. Tektronix ships updated and tested exchange boards. Each board comes with a 90-day service warranty.

For More Information. Contact your local Tektronix service center or sales engineer for more information on any of the calibration and repair services.

Service Options

Tektronix offers the following service options. These options are modular, flexible, and easy to order with your instrument. Designed to ease installation and startup, to support tracking of calibration to requirements of ISO9000, and to provide for extended repair coverage, these options help fix your long-term maintenance costs and eliminate unplanned expenditures. These options can be converted from service at Tektronix service depots to service on-site (see Option S1 and S3), which helps keep downtime to a minimum.

TLA600 Series Service Options

The following service options are available for your TLA600 series logic analyzer.

Three years repair coverage	Option R3	Extends product repair warranty to a total of three years.
Three years of calibration services	Option C3	Provides factory calibration certification on delivery, plus two more years of calibration coverage. Throughout the coverage period the instrument will be calibrated according to its Recommended Calibration Interval.
Test data	Option D1	Provides initial Test Data Report from factory on delivery.
Test data	Option D3	Provides test data on delivery plus a Test Data Report for every calibration performed during 3 years of coverage – requires Option C3.

TLA700 Series Service Options

The following service options are available for your TLA700 series logic analyzer.

Three years repair coverage	Option R3	Extends product repair warranty to a total of three years.
One year upgrade to on-site service ^{1,2}	Option S1	Upgrades the standard one year, “return to depot” warranty to an on-site warranty.
Three year upgrade to on-site service ^{1,2}	Option S3	Upgrades any C3, D3, and R3 options purchased to on-site coverage for three years.
Three years of calibration services	Option C3	Provides factory calibration certification on delivery, plus two more years of calibration coverage. Throughout the coverage period the instrument will be calibrated according to its Recommended Calibration Interval.
Test data	Option D1	Provides initial Test Data Report from factory on delivery.
Test data	Option D3	Provides test data on delivery plus a Test Data Report for every calibration performed during 3 years of coverage – requires Option C3.
Product installation service	Option IN	Provides initial product installation/configuration and start-up training session including front panel and product familiarization.

¹ Availability of installation and on-site services depends on the type of product and may vary by geography.

² Upgrade options are ordered with the mainframe products and cover individual modules.

General Care

Protect the instrument from adverse weather conditions. The instrument is not waterproof.

Do not store or leave the instrument where the LCD display will be exposed to direct sunlight for long periods of time.



CAUTION. To avoid damage to the instrument, do not expose it to sprays, liquids, or solvents.

Module Self Calibration

Use the Self Calibration property page to run self calibration procedures for installed modules and merged modules. For all modules, you should run these procedures after repair. At a minimum, you should run these procedures once a year. For the DSO module you should also run these procedures if the ambient operating temperature has changed more than 5°C since last calibration or once a week if vertical settings of 50 mV full scale or less are used.

Perform self calibration after a 30 minute warm up.

- To run the self-calibration procedure, go to the System menu and select Calibration and Diagnostics. Click Self Calibration.

NOTE. For merged modules, run the self-calibration procedure on the modules as a merged set.

Preventive Maintenance

Once a year the electrical performance should be checked and the instrument accuracy certified (calibrated). This service should be performed by a qualified service technician using the procedures outlined in the *Tektronix Logic Analyzer Family Performance Verification and Adjustment Technical Reference Manual*.

Preventive maintenance mainly consists of periodic cleaning. Periodic cleaning reduces instrument breakdown and increases reliability. Clean the instrument as needed, based on the operating environment. Dirty conditions may require more frequent cleaning than computer room conditions.

Flat Panel Display Cleaning

The LCD flat panel is a soft plastic display and must be treated with care during cleaning.



CAUTION. *Improper cleaning agents or methods can damage the flat panel display.*

Do not use abrasive cleaners or commercial glass cleaners to clean the display surface.

Do not spray liquids directly on the display surface.

Do not scrub the display with excessive force.

Clean the flat panel display surface by gently rubbing the display with a clean-room wipe (such as Wypall Medium Duty Wipes, #05701, available from Kimberly-Clark Corporation).

If the display is very dirty, moisten the wipe with distilled water or a 75% isopropyl alcohol solution and gently rub the display surface. Avoid using excess force or you may damage the plastic display surface.

Exterior Surfaces

Clean the exterior surfaces with a dry, lint-free cloth or a soft-bristle brush. If dirt remains, use a cloth or swab dampened with a 75% isopropyl alcohol solution. A swab is useful for cleaning in narrow spaces around the controls and connectors. Do not use abrasive compounds on any part of the instrument.



CAUTION. *Avoid getting moisture inside the instrument during external cleaning; and use only enough solution to dampen the cloth or swab.*

Do not wash the front-panel On/Standby switch. Cover the switch while washing the instrument.

Use only deionized water when cleaning. Use a 75% isopropyl alcohol solution as a cleanser and rinse with deionized water.

Do not use chemical cleaning agents; they may damage the instrument. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Floppy Disk Drive

The floppy disk drive requires routine maintenance to operate at maximum efficiency. The disks can be damaged if dirt and dust accumulate on the recording surfaces. To prevent damage, the disks should be properly stored in their protective containers where they will not be exposed to dust or dirt. In addition, the head should be cleaned periodically.

You will need a 3.5-inch floppy disk head-cleaning kit for routine maintenance. Perform the routine maintenance as follows:

- Clean the face of the floppy disk drive monthly with a dampened cloth.



CAUTION. Do not allow moisture to enter the disk drive. When power is applied, the internal components can be damaged.

- Clean the head monthly. Follow the instructions provided with the head-cleaning kit.

In Case of Problems

This section provides information to help you address problems you may encounter while installing and using your logic analyzer.

Diagnostics

The logic analyzer runs power-on diagnostics every time you power on the instrument. You can view the results of the diagnostics by selecting Calibration and Diagnostics from the System menu. You can run more detailed diagnostics by selecting Extended diagnostics. Here you can run all tests, loop on one or more tests, or loop on a test until a failure occurs.

The following diagnostic tools are available with your logic analyzer:

Power-On Diagnostics. Power-on diagnostics run when you first turn on the logic analyzer, or when you first start the TLA or the pattern generator application. If any diagnostic failures occur during turn on, the Calibration and Diagnostics property page appears.

Extended Diagnostics. Extended diagnostics test the logic analyzer more thoroughly than the power-on diagnostics. The extended diagnostics test the modules in the benchtop mainframe as well as the modules in the expansion mainframe(s). You can use the extended diagnostics to isolate problems to an individual module.

Before running the extended diagnostics, disconnect any attached probes.

NOTE. Some items in the extended diagnostics menu will fail if a LA module, DSO module, or pattern generator module is running. Stop all modules before performing the extended diagnostics.

TLA700 Mainframe Diagnostics. The TLA mainframe diagnostics program is a stand alone Windows application. These diagnostics check operation of the mainframe beyond the basic PC circuitry. These diagnostics also check the front panel knobs of the portable mainframe.

Expansion Mainframe Diagnostics. At power-on, the expansion mainframe runs two power-on diagnostics: “Power, Cables A & B and config”, and “Cable C Connection Test”.

If either of these power-on diagnostics fail, none of the modules associated with the expansion mainframe, and possibly the expansion mainframe itself, will be recognized. The result will be as if the expansion mainframe was not connected.

Turn off the mainframes. Remove the two blue expansion cables and the gray expansion cable. Examine the connectors for bent or missing pins. Reconnect the two blue expansion cables and the expansion cable, and tighten the two connector screws. Turn on the mainframes and try again.

QA+Win32 Diagnostics. The QA+Win32 diagnostics is a separate Windows application located in the Windows Start Programs menu. The diagnostics check the basic operation of the controller.

Software Problems

Your logic analyzer comes with most software installed. Before running any of the diagnostics, you should check the online release notes to verify the logic analyzer software is compatible with the module firmware.

Run the QA+Win32 diagnostics software to identify hardware or software problems. Follow the QA+Win32 online help instructions for running the diagnostics software. The diagnostics are located in the Start menu at:

\Programs\QA+Win32

Many software problems can be due to corrupted or missing software files. In most cases the easiest way to solve software problems is to reinstall the software and follow the on-screen instructions. Refer to *Upgrading Software* for instructions on reinstalling or upgrading software.

Refer to Table H–1 on page H–8 for a list of software and hardware troubleshooting information and recommended action. Note that this table can be used to identify problems for the entire Tektronix logic analyzer family.

If you suspect problems with the application software, contact your local Tektronix representative.

Hardware Problems

If you are certain that you have installed the logic analyzer correctly, run the extended diagnostics (located under the System menu) to identify any problems.

If your logic analyzer powers up so that you have access to the desktop, run the QA+Win32 diagnostics software to identify possible controller hardware problems. Follow the QA+Win32 online help instructions for running the diagnostics software. The diagnostics are located in the Start menu.

You can also run the external TLA mainframe diagnostics to identify problems not covered by other diagnostics. The TLA mainframe diagnostics are located under the Start menu under the Tektronix Logic Analyzer programs.

Check for Common Problems

Use Table H-1 to help isolate problems. This list is not exhaustive, but it may help you eliminate problems that are easy to fix, such as an open fuse, loose cable, or defective module (TLA700 series).



CAUTION. Do not install or remove any modules while the instrument is turned on. Installing or removing modules when the instrument is turned on can damage any installed modules and the mainframes.

Table H-1: Failure symptoms and possible causes

Symptom	Possible causes and recommended action
Instrument does not turn on	<p>Verify that all power cords are connected to the instrument and to the power source.</p> <p>Check that the instrument receives power when you press the On/Standby switch.</p> <p>Check that fans start and that front-panel indicators light.</p> <p>Check that power is available at the power source.</p> <p>Check for failed fuses.</p> <p>Instrument failure: contact your local Tektronix service center.</p>
Expansion mainframe does not turn on	<p>Verify that all power cords are connected to the expansion mainframe and to the power source.</p> <p>Check that all of the expansion modules are firmly seated, and that the mounting screws on the expansion modules are tightened.</p> <p>Check that the cables between the mainframe and the expansion mainframe are correctly connected: A → A, B → B, and C → C.</p> <p>Check that the expansion module is in slot 0 of the expansion chassis.</p> <p>Check that power is available at the power source.</p> <p>Check for failed fuses.</p> <p>Expansion mainframe failure: contact your local Tektronix service center.</p>

Table H-1: Failure symptoms and possible causes (Cont.)

Symptom	Possible causes and recommended action
Monitor does not turn on	<p>Check the monitor power cord connection.</p> <p>Check for failed fuse.</p> <p>Monitor failure: contact the vendor of your monitor for corrective action.</p>
Monitor display is blank	<p>Check that the monitor is connected to the mainframe; replace the cable if necessary.</p> <p>If instrument display is blank, try connecting external monitor; if both displays are blank, contact your local Tektronix service center.</p> <p>External monitor controls turned down; adjust monitor controls for brightness and contrast.</p> <p>Check the controller BIOS setups for the monitor.</p> <p>Faulty monitor; contact the vendor of your monitor for corrective action.</p>
Instrument turns on but does not complete the power-on sequence	<p>If the instrument is a TLA 700 series, turn off the instrument and check that all of the modules are fully inserted.</p> <p>If the mainframe is a benchtop mainframe, check the status of the SYSTEM FAIL and TEST LEDs on the benchtop controller. If either LED stays on, contact your local Tektronix service center.</p> <p>Check the status of the READY and ACCESSED LEDs on the front panel of the application modules. The READY LED turns on when the module passes the power-on diagnostics and when the module is ready to communicate with the controller. The ACCESSED LED turns on any time the controller accesses the module.</p> <p>Check for disk in floppy disk drive; make sure mainframe boots from the hard disk drive.</p> <p>Check for faulty module. Remove modules one at a time and turn on the instrument. If the instrument completes the power-on sequence, replace the faulty module.</p> <p>Possible software failure or corrupted hard disk; see <i>Software Problems</i> at the beginning of this chapter.</p>
Power-on diagnostics fail	<p>Isolate problem to a faulty mainframe or to a faulty module. Multiple diagnostic failures across modules indicate a faulty mainframe. Diagnostic failures confined to an single module most likely indicate a faulty module. Contact your local Tektronix service center.</p>
Instrument does not recognize accessories such as monitor, printer, or keyboard	<p>Check that accessories are properly connected or installed. Try connecting other standard PC accessories or contact your local Tektronix service center.</p>
LA Module merge not allowed in TLA700 Application	<p>Merge cable between LA modules not installed.</p> <p>LA modules are not compatible: TLA7Nx and TLA7Px LA modules may not be merged with TLA 7Lx and TLA7Mx LA modules.</p> <p>Refer to the Merge Rules on page E-1.</p>
Windows comes up but the TLA or pattern generator application does not	<p>Instrument not set up to start the TLA application at power-on. Start application from the desktop, by double-clicking on the TLA Final Setup icon located on your desktop.</p> <p>Faulty or corrupt software. Reinstall the application software.</p>

Table H-1: Failure symptoms and possible causes (Cont.)

Symptom	Possible causes and recommended action
Windows comes up in Safe mode	<p>Exit the Safe mode and restart the instrument.</p> <p>Incompatible hardware and hardware driver software. Either install hardware driver or remove the incompatible hardware.</p>
Application starts but modules do not display in System window	<p>Module firmware has not been updated.</p> <p>The flash jumper was not removed after the module firmware was updated.</p> <p>Turn off instrument off and check that all modules are fully inserted.</p> <p>Module address switches not set correctly. Turn the instrument off and remove module. Set address switches to FF and reinstall module (refer to Figure G-1 on page G-15 for address switch locations).</p> <p>Module failure; replace with known-good module or contact your local Tektronix service center.</p> <p>Instrument failure; contact your local Tektronix service center.</p> <p>Automatic merging sometimes looks like a missing module.</p>
<p>Expansion mainframe is not recognized by the system.</p> <p>Expansion mainframe does not show up in the system window.</p>	<p>Note: If there is no DSO or LA module installed in the expansion mainframe, the expansion mainframe will not show up in the System window. If modules are installed, follow these instructions:</p> <p>Turn off the mainframe(s).</p> <p>Check that both of the TLA7XM expansion modules are firmly seated, and that the mounting screws on the TLA7XM expansion modules are tightened.</p> <p>Remove the two blue expansion cables and the gray expansion cable. Examine the connectors on the cables for bent or broken pins. Examine the connectors on the expansion mainframe.</p> <p>Reconnect the two blue expansion cables and the gray expansion cable and tighten the screws on the connectors. Verify that the cables are not crossed; verify that the cables are connected: A → A, B → B, and C → C.</p> <p>Power on the benchtop mainframe and the expansion mainframe(s). (The mainframe power must be recycled in order for the ResMan32 (resource manager) application to correctly configure.)</p> <p>Expansion mainframe failure; contact your local Tektronix service center.</p>
Expansion mainframe is recognized by the system, but installed modules are not.	<p>Turn off the benchtop mainframe.</p> <p>Turn on the benchtop mainframe. The mainframe power must be recycled in order for the ResMan32 (resource manager) application to correctly configure.</p> <p>Module address switches not set correctly. Turn off the benchtop mainframe and remove the module(s) from the expansion mainframe. Set address switches to FF and reinstall module (refer to Figure G-1 on page G-15 for address switch locations).</p> <p>Turn off the benchtop mainframe, install a known good module from the benchtop mainframe into the expansion mainframe (the expansion mainframe where the modules were not recognized). Turn on the benchtop mainframe and retry.</p> <p>Module failure; contact your local Tektronix service center.</p>

Table H-1: Failure symptoms and possible causes (Cont.)

Symptom	Possible causes and recommended action
Portable mainframe will not turn off with On/Standby switch.	<p>The mainframe utilities may be set up to disable hard power-off. Check the setting of the mainframe utilities (the mainframe utilities are located in the Windows Control Panel).</p> <p>This is a Windows operating system problem. Try turning off the instrument using the Windows shutdown procedure. If the instrument still does not turn off, disconnect power cord and reconnect after 10 seconds to reboot the instrument.</p>
Expansion Mainframe will not turn off with On/Standby switch.	<p>If the expansion mainframe was incorrectly shut down (for example, the power cord was disconnected while the expansion mainframe was running), the expansion mainframe utility still registers the expansion mainframe as in the powered on condition.</p> <p>To correct this condition, press and hold the expansion mainframe power switch for three to four seconds. The expansion mainframe will turn off on its own. Power off the benchtop mainframe. Power on the benchtop mainframe; the expansion mainframe will turn on normally.</p>

Startup Sequence

The following information is intended to provide troubleshooting hints in case the logic analyzer fails to complete the startup sequence. Refer to Figure H-1 on page H-12 while reading the following paragraphs.

At power-on, the mainframe software starts the mainframe and module kernel tests. If the mainframe passes the kernel tests, it attempts to boot the Windows operating system. If the mainframe fails the kernel tests, it displays the error code(s), beeps, and terminates the startup sequence.

The Windows operating system starts the resource manager. The resource manager (ResMan32) performs the following tasks:

- Runs mainframe power-on self tests.
- Runs expansion mainframe power-on self tests.
- Verifies the power-on self test status.
- Inhibits any failed modules.
- Records the power-on self test failures.
- Determines the logic analyzer configuration.
- Executes the system controller power-on diagnostics.

After completing all of the above tasks, the logic analyzer starts the TLA application which performs the following tasks:

- Runs power-on diagnostics on all installed modules.
- Runs power-on diagnostics on the TLA system.
- Records the Pass/Fail status in the Calibration and Diagnostics property sheet.

If no failures occur, the application is ready to use for regular tasks.

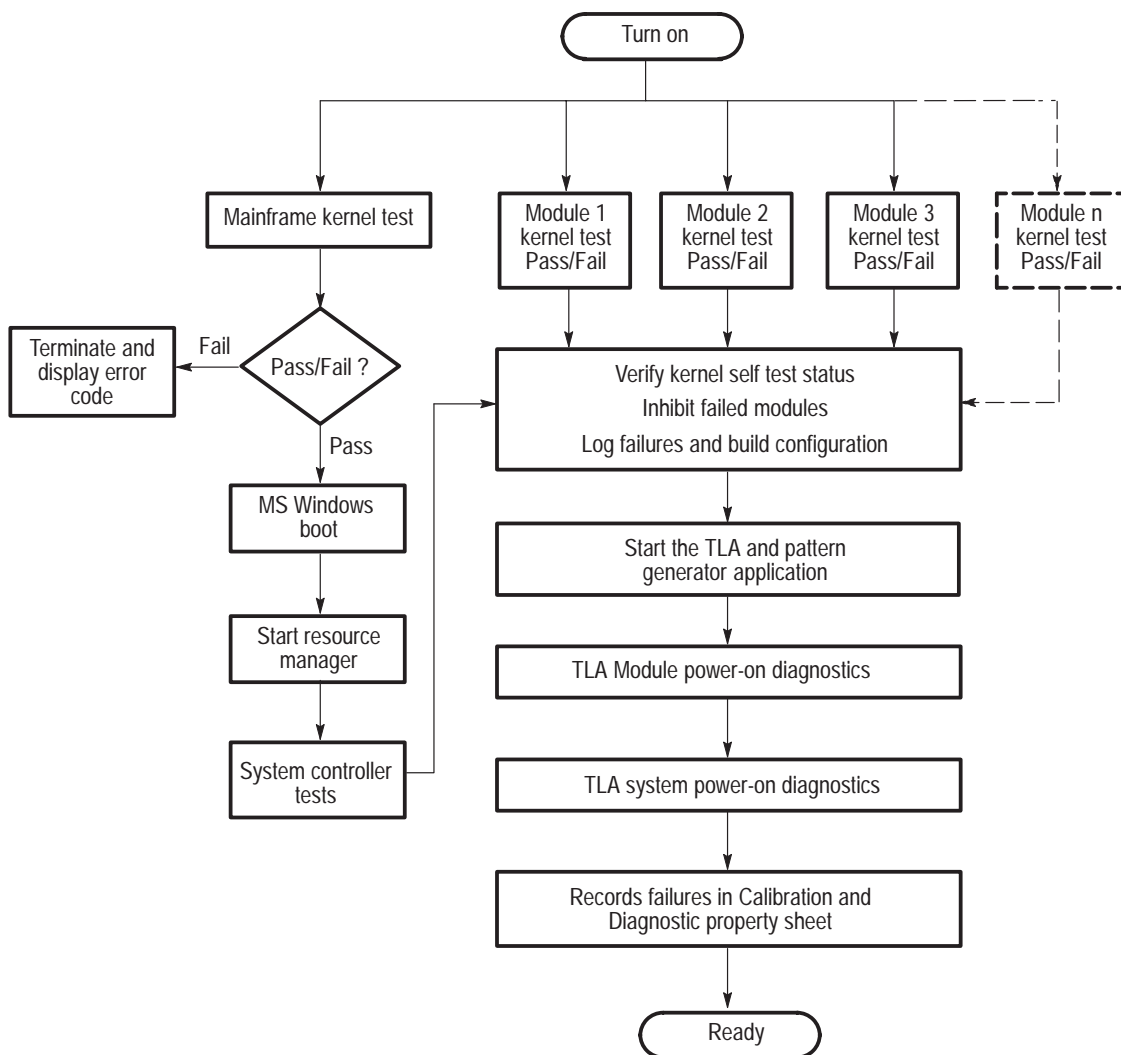


Figure H-1: TLA startup sequence

Isolating Problems

If you have completed all of the troubleshooting procedures up to this point and the application fails to display any modules in the System window, you may have a system problem. Although most of the following steps apply to the TLA 700 series, some of the steps may also be helpful in identifying problems with the TLA 600 series.

- Verify that all modules are properly installed in the mainframe.
- Verify that the module address switches are set correctly. Power off the instrument and remove the modules. Set the address switches to FF and reinstall the modules.
- Verify that the modules do not have the flash programming jumper installed on the rear of the module. Power off the instrument and remove the modules. Remove the jumper and reinstall the modules.
- Try placing a suspected module in a different slot to verify slot dependency problems. For example, if you have a module in one set of slots, power off the instrument, move the module to a different set of slots, and then try the tests again. If the module works in the new location, you have identified a faulty slot in the instrument.
- Check for bent or broken pins on the backplane of the instrument.

You can execute the internal resource manager program (ResMan32.exe) to identify if any of the installed modules are being identified in the instrument slots. Table H-2 lists some of the command line options for executing the ResMan32 software.

Table H-2: Command line options for ResMan32

Option	Description
-a, -A, -o, -O	ResMan32 will not close the text window after executing and displaying the results the major functions (default).
-p, -P	ResMan32 will not execute the mainframe power-on self test diagnostics (default).
-v, -V	ResMan32 records the resource manager actions in the text window in a short form or nonverbose mode.
+a, +A, +o, +O	ResMan32 will terminate the tests and display the resultant action information in the text window.
+p, +P	ResMan32 will perform the mainframe power-on self test diagnostics.
+v, +V	ResMan32 records all actions in a text window in the verbose mode (default).

Table H-2: Command line options for ResMan32 (Cont.)

Option	Description
+t, +T	ResMan32 will not display the text window and the tests will terminate after executing regardless of the error conditions.
+m, +M	ResMan32 displays in a minimized window.

Complete the following steps to start the ResMan32 software:

1. Exit all applications.
2. Click the Windows Start button and select Run.
3. In the dialog box enter the following path:

C:\Program Files\TLA700\System\ResMan32.exe

4. Click OK.

The ResMan32 (resource manager) program will check all of the installed modules and their address locations. The program will print out data similar to that in Figure H-2. In this example the mainframe has two logic analyzer modules installed.

If resource manager encounters any errors (such as an unsupported module), the resource manager will stop further communications and display information on why or at what point the module was disabled.

```
#Resource Mgr
#09/09/97 08:48:49
Auto Exit - Off
Identify Static Configure Devices
    Found a device at LA 1
    Found a device at LA 2
Identify Dynamic Configure Devices
Matching Devices to Slots
    match la=1 to slot=1
    match la=2 to slot=3
Setting VISA Attributes
    la 1, slot 1: device_class 2, manf_id 0xffd, model_code 0x7f4, addr_spc 0
    la 2, slot 3: device_class 2, manf_id 0xffd, model_code 0x7f1, addr_spc 0
Setting VISA Address Maps
    A24 device @ la 1 - starting address 200000x, size 65536
    A24 device @ la 2 - starting address 210000x, size 65536
Enabling Events & Responses
    la 1: Int ID 1 assigned to IRQ 4
    Enabling Events: 16-32 124-125 127
    la 1: Asynchronous Enable succeeded
        **Responses are unsupported by this device
    la 2: Int ID 1 assigned to IRQ 4
    Enabling Events: 16-32 124-125 127
    la 2: Asynchronous Enable succeeded
        **Responses are unsupported by this device
Begin Normal Operation
```

```

slot 1, LA 1, started successfully
slot 3, LA 2, started successfully
VISA Data
  la_1=1,1,4093,2036,2,0,1,7,2097152
  la_2=2,3,4093,2033,2,0,1,7,2162688

```

Figure H-2: Example ResMan32 program output

Expansion Mainframe Problems

Because the expansion mainframe adds a level of complexity to troubleshooting problems, this section will concentrate on tips to aid you in troubleshooting expansion mainframe related problems.

If you have exhausted all of the failure symptoms and possible causes listed Table H-1 beginning on page H-8, try some of the following tips.

Look and Listen for the Expansion Mainframe Power-On Sequence. There are certain signs that the expansion mainframe is not powering up correctly. By looking and listening to these signs you can determine if the expansion mainframe is not powering up due to missing signals from the expansion module.

Upon powering up the benchtop mainframe, the expansion module sends a signal from the benchtop mainframe to the expansion module in the expansion mainframe via the three expansion cables. If the expansion mainframe does not receive this signal, the expansion mainframe will not power up.

If the power on signal is received by the expansion mainframe, the fan starts and the lamp on the mainframe lights. Further indications that the mainframe receives signals from the expansion module are blinking lights on the expansion module and on other installed modules.

Substitute a Known Good Expansion Module. If you have a known good expansion module, try the following procedure:

1. Verify that the expansion module is installed in slot 0 and that the logical address switches on the back of the module are set to FF.
2. Try swapping the expansion module from the benchtop mainframe with the expansion module from the expansion mainframe. This sometimes works because one module is a sender while the other module is a receiver.



CAUTION. *The single-wide expansion module requires up to 60 lbs. of insertion force to engage it into the back plane. Do not use the mounting screws to engage the module into the backplane of the chassis.*

The mounting screws will not provide enough force to seat the expansion module, and you can easily strip the threads.

3. Install the known good expansion module in slot 0 of the expansion chassis.
4. Power on the benchtop mainframe and check for normal operation.
5. If the failure symptoms are still present with the known good expansion module, the problem is most likely in the expansion mainframe.
6. If your expansion mainframe operates normally with the known good expansion module, then the suspect expansion module needs to be serviced.

Check the Expansion Mainframe. If you do not have a known good expansion module, perform the following procedure:

1. Remove all modules from the expansion mainframe except the for the expansion module.
2. Power on the benchtop mainframe and determine if the expansion mainframe is recognized by the instrument.

Replace the Expansion Module with a Benchtop Controller Module. Make the expansion mainframe simulate a benchtop mainframe. Do this by removing the expansion module from the slot 0 position in the expansion mainframe and replacing it with a known good benchtop controller module from the benchtop mainframe.

Because the expansion mainframe is set up to power on from a signal from the expansion module (which is no longer present) you need to press the On/Standby switch on the expansion mainframe.

If the expansion mainframe powers on correctly, the problem can be isolated to either the expansion module(s) or to the expansion cable(s).

Repacking for Shipment

If a mainframe or module is to be shipped to a Tektronix field office for repair, attach a tag to the mainframe or module showing the owner's name and address, the serial number, and a description of the problem(s) encountered and/or service required. If you return a module, always include the module and the probes so that the entire unit can be tested.

When packing an instrument for shipment, use the original packaging. If it is unavailable or not fit for use, contact your Tektronix representative to obtain new packaging.



Glossary

Glossary

AC coupling

A DSO mode that blocks the DC component of a signal but passes the dynamic (AC) component of the signal. Useful for observing an AC signal that is normally riding on a DC signal.

Acquisition

The process of sampling signals from input channels, processing the results, and displaying the data.

Active module

The module highlighted by the pointer in the System window.

Aliasing

The condition that occurs when data is sampled at a rate slower than the rate at which data changes. When this happens, misleading data is displayed because the instrument misses the changes in data that occurred between sample points. Data pulses that fall between samples meet the technical definition of a glitch and are stored and displayed as glitches. See also *asynchronous acquisition* and *glitch*.

For DSO data, the displayed waveform may appear to be untriggered and much lower in frequency. For complex waveforms, distortion occurs due to the impact of aliasing on the high-order harmonics.

All samples

A Histogram window term. The total number of data samples analyzed.

Arm

To specify when the module should begin looking for a trigger.

Assert

To cause a signal or line to change from its logic false state to its logic true state.

Asynchronous acquisition

An acquisition that is made using a clock signal generated internally by the logic analyzer. This clock is unrelated to the clock in the system under test, and you can set it to a different rate. You should use an asynchronous clock rate that is five to ten times faster than your data rate to avoid aliasing. See also *Aliasing*.

Attenuation

The degree the amplitude of a signal is reduced when it passes through an attenuating device such as a DSO probe or attenuator (the ratio of the input measure to the output measure). For example, a 10X probe attenuates, or reduces, the input voltage of a signal by a factor of 10.

Benchtop Chassis

A benchtop chassis is a benchtop mainframe without a benchtop controller installed.

Chassis

A chassis is a mainframe without a controller or expansion module installed.

Clause

A trigger program term. The combination of one or more events (If statements) or actions (Then statements). When the Event is satisfied, the action is performed. See also *State*.

Clock cycle

A clock sequence that includes both high- and low-going transitions.

Clock equation

The Boolean combination of events needed to generate a storage clock. You can define a variety of clock inputs and link them using Boolean operators. Data will be sampled and stored in memory only when this clock equation is true.

Clock qualification

The process of filtering out irrelevant data by combining an acquisition clock with one or more bus signals.

Clock qualifier

An external signal that acts as a gate for the acquisition clock. When the external signal is false, the acquisition clock is not allowed to load acquired data into the acquisition memory.

COFF file formats

The COFF (Common Object File Format) format contains a number of variations and extensions, such as ECOFF and XCOFF. This flexibility enables it to be used with a wide variety of different microprocessors. Some code-generation tool vendors also extend this format in nonstandard ways that may make their files unreadable by the TLA logic analyzers.

Color range symbols

Color range symbols define the beginning and ending group values where color is displayed.

Counter

A trigger program device that records occurrences of an event.

Cursors

Paired markers that you can use to make measurements between two data locations.

Custom clocking

Custom clocking is used only with microprocessor support packages. Custom clocking can enable and disable a variety of microprocessor-specific clock cycle types (such as DMA cycles).

Data differences

Highlighted data in a Listing or Waveform window that indicate that there are differences between the acquired data and saved data during a compare operation.

Data equalities

Highlighted data in a Listing or Waveform window that indicate that there are no differences between the acquired data and saved data during a compare operation.

Data sample

The data logged in during one occurrence (or one cycle) of the acquisition clock. A data sample contains one bit for every channel.

Data window

A window used to display acquired data. There are two types of data windows, Listing windows and Waveform windows.

DC coupling

A DSO mode that passes both AC and DC signal components to the DSO circuit. Available for both the trigger system and the vertical system.

Delta measurement

The difference between two points in memory. For example, the voltage difference between the two cursors in a selected waveform.

Demultiplex

To identify and separate multiplexed signals (for instance, some signals from a microprocessor). To separate different signals sharing the same line and organize those signals into useful information.

Digital real-time signal acquisition

A digitizing technique that samples the input signal with a sample frequency of four to five times the DSO bandwidth. Combined with $\sin(x)/x$ interpolation, all frequency components of the input up to the bandwidth are accurately displayed.

Digitizing

The process of converting a continuous analog signal such as a waveform to a set of discrete numbers representing the amplitude of the signal at specific points in time.

Don't care

A symbol (X) used in place of a numeric character to indicate that the value of a channel or character is to be ignored.

Edge

A signal transition from low to high, or high to low.

Edge trigger

Triggering that occurs when the module detects the source passing through a specified voltage level in a specified direction (the trigger slope).

Event condition

Event conditions are a logical combination of trigger events within a single clause. If you set up a logical AND statement, all event conditions in the clause must be fulfilled before the clause can execute the action. If you set up a logical OR statement, any one of the event conditions can be fulfilled before the clause can execute the action.

Expansion Chassis

An expansion chassis is an expansion mainframe without an expansion module installed.

External clock

A clock external to the logic analyzer and usually synchronous with the system under test.

Internal signal

An internal communication line that can be set as a marker. An internal signal can be used as either an event or an action in a trigger program. When used as an event, the internal signal is tested for true/false value like any other event; when used as an action, the signal can simply be set or cleared as the result of a condition being satisfied.

Glitch

An unintentional signal that makes a transition through the threshold voltage two or more times between successive sample clock cycles. Noise spikes and pulse ringing are examples of glitches.

Ground (GND) coupling

A DSO coupling option that disconnects the input signal from the vertical system.

Histogram window

A data window used to observe the performance of software routines.

IEEE695 file format

This object file format refers to the IEEE695 specification. This format is used primarily by compilers for a wide variety of Motorola microprocessors and compatible microprocessors from other vendors. This format provides for the inclusion of column information in source symbols, but not all compilers use this capability.

Internal clock

A clock mode in which the sampling of input logic signals occurs asynchronously to the activity of the system under test.

Interpolation

Display method used to connect the sample points acquired and display them as a continuous waveform. The logic analyzer uses $\sin(x)/x$ interpolation to display DSO signals.

Linear generation

A Histogram window term. The histogram ranges are evenly distributed from the highest range boundary to the lowest range boundary.

Listing window

A data window used to observe the data flow in the system under test. The acquired data is displayed in a listing (tabular text) format.

Log generation

A Histogram window term. The histogram ranges are distributed over a logarithmic scale.

MagniVu data

High-speed data stored in a special memory.

Matched samples

A Histogram window term. The total number of data samples analyzed that matched a defined range. These samples exclude any samples outside of the defined ranges.

Merge modules

To physically or logically join LA modules together to form a single module with greater channel width.

Microprocessor support

Optional microprocessor support software that allows the logic analyzer to disassemble data acquired from microprocessors.

Mnemonic disassembly

A display format for data acquired from a microprocessor or a data bus. A logic analyzer decodes bus activity and displays it in formats such as: cycle types, instruction names, and interrupt levels. Advanced forms of mnemonic disassembly can detect queue flushes, and provide a display that resembles the original assembly language source code listing.

Module

The unit that plugs into a mainframe, providing instrument capabilities such as logic analysis.

Module trigger (trigger)

A trigger specific to a single module. When a module trigger occurs, the module continues to acquire data until the specified amount of posttrigger data is acquired, and then stops.

OMF51 file format

This format holds symbolic information and executable images for a 8051 or equivalent microprocessor.

OMF86 file format

A file format that holds symbolic information and executable images for an 8086 or equivalent microprocessor. It is also used for code intended to run on 80286, 80386, or higher-level microprocessors in real or 8086-compatible mode.

OMF166 file format

This format holds symbolic information and executable images for the Siemens (Infinion) C166 microprocessor family, or equivalent microprocessor.

OMF286/386 file formats

These file formats hold symbolic information and executable images for 80286 80386, or equivalent microprocessors. They are also used for executable images intended to run on the 8086 or other microprocessors in the 80x86 families.

PCMCIA

An acronym for Personal Computer Memory Card Industry Association.

Podlet

A circuit contained in a flex lead and attached to a probe that provides square-pin connections to the circuit under test for one data acquisition channel and a ground pin.

Pretrigger

The specified portion of the data record that contains data acquired before the trigger event.

Post trigger

The specified portion of the data record that contains data acquired after the trigger event.

Probe adapter

A microprocessor-specific lead set that connects the LA module probe to a system under test.

Qualification gap

Qualification gaps indicate that data samples were not stored due to storage qualification or Don't Store trigger actions. In a Listing window, qualification gaps are indicated by a horizontal gray line. In a Waveform window, qualification gaps are indicated by a blank vertical gap.

Range recognizer

A trigger term. Use range recognizers to trigger the logic analyzer on ranges of data.

Record length

The specified number of samples in an acquisition.

Sample clock

The clock signal that determines the points in time when the module samples data. A sample clock can be set up to occur at regular intervals specified by an internal clock (asynchronous acquisition), or to occur when a Boolean expression combining an external clock and qualifier signals is "true" (synchronous acquisition).

Sample rate

The frequency at which data is logged into the logic analyzer.

Sampling

The process of capturing an input signal, such as a voltage, at a discrete point in time and holding it constant so that it can be quantized.

Skew

The relative time difference between input channels, specified in terms of one edge relative to another. Also, the misrepresentation of data caused by parallel channels with different propagation delays.

Source Window

A data window where you can view the execution of source code.

Standby (STBY)

The off-like state when the instrument is not in use. Some circuits are active even while the instrument is in the standby state.

State

A trigger program term. A step in a trigger program, made up of one or more clauses. See also *clause*.

Storage qualification

The process of filtering out data that has been acquired but which you do not want to store in acquisition memory. This allows you to avoid filling up your module's acquisition memory with irrelevant data samples.

Symbolic range generation

A Histogram window term. The histogram ranges are defined in a range symbol file. The highest and lowest ranges depend on the maximum and minimum boundaries for the ranges defined in the symbol file.

Symbolic radix

A format that allows you to substitute mnemonics (names) for radix numbers in the Trigger and data windows.

Synchronous acquisition

An acquisition that is made using a clock signal generated external to the logic analyzer. This clock is usually the clock in the system under test. The external clock is usually synchronous with the system under test and may or may not be periodic.

System trigger (trigger all)

An overriding command to all modules that causes them to stop looking for a trigger, and to acquire their posttrigger data, regardless of whether they have been armed or have fulfilled their own trigger conditions. The system trigger also functions as the primary reference point for the entire data acquisition. In data windows, timing and location information is relative to the system trigger.

Time correlation

The tracking of independent events captured by different modules and indicating how they relate to each other in time. Specifically, the chronological interleaving of data from different modules into a single display. Shows real-time interactions between independently clocked circuits.

Time stamp

A separate clock value stored with each acquisition cycle.

Timer

A trigger program device that records elapsed time.

Threshold voltage

The voltage to which the input signals are compared.

Trigger

An event or condition that leads to the end of an acquisition cycle. When started, the instrument continuously acquires data from a system under test until the trigger occurs. After triggering, the instrument continues to acquire data until the post-fill requirement is met.

Trigger library

A collection of predefined trigger programs for the LA module. You can load an individual program into the Trigger window and modify it for your requirements.

Trigger position

Where the trigger resides in acquisition memory. Electing to place the trigger in the center of memory means that half of the acquisition consists of data that occurred after the trigger.

Trigger program

A series of conditions, similar to software code, that defines the data you want to capture and view. The trigger program also specifies actions for data events. The trigger program filters acquired data to find a specific data event or series of data events. The trigger program can accept information from other modules or send signals external to the logic analyzer.

TSF

TLA Symbol File (TSF) format (a text format). The TSF format is used by the logic analyzer when it exports symbol files.

Unassert

To cause a signal or line to change from its logic true state to its logic false state.

Waveform window

A data window used to observe timing relationships in the system under test. The acquired data is displayed as a series of waveforms.

Word recognizer

A trigger term. Word recognizers are specific patterns of data or words. Use word recognizers to trigger the logic analyzer on specific data combinations.



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