Reference

Tektronix

Fully Buffered DIMM (FB-DIMM)

Methods of Implementation (MOI)

071-1773-00

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- Worldwide, visit www.tektronix.com to find contacts in your area.

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1 Introduction to RT-Eye FB-DIMM Compliance Module

This document provides the procedures for making FB-DIMM compliance measurements with Tektronix TDS6604B, **TDS6804B**, TDS7704B, **TDS6124C**, and **TDS6154C** oscilloscopes. The FB-DIMM Compliance Module (**Opt. FBD**) is an optional software plug-in to the RT-Eye Serial Data Compliance and Analysis application (**Opt. RTE-Version 2.0**). The FB-DIMM Compliance Module provides amplitude, timing, and jitter measurements described in Section 3 of Revision 0.7 of the FB-DIMM Draft Specification dated May 10, 2005. (For Compliance testing of FB-DIMM signals (3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s) a minimum oscilloscope BW of 12 GHz is required. Using an 8 GHz BW oscilloscope, you can test the 3.2 GB/s FB-DIMM signals for compliance)

All references to the Draft Specification are to Revision 0.7 of the FB-DIMM Draft Specification. In the subsequent sections, step-by-step procedures are described to help you perform FB-DIMM measurements. Each measurement is described as a Method of Implementation (MOI). For further information, refer the Compliance checklists offered to JEDEC members at www.jedec.org.

2 FB-DIMM Compliance Measurements

Electrical Specifications for FB-DIMM are provided in Section 3 of the Draft Specification. Most of the measurements are available in the FB-DIMM Compliance Module.

2.1 Common Specifications between Transmitter and Receiver

The TX and RX PLLs shall obey the bandwidth and jitter peaking specifications in the following table for continuous transmission operation.

Table 1: PLL Specification for TX and RX

Symbol	Parameter	Min	Max	Units	Notes
$F_{PLL\text{-}BW\_TX\text{-}RX}$	-3dB bandwidth	11	33	MHz	1
$JitPk_{TX\text{-}RX}$	Jitter Peaking		3	dB	2

NOTES:
1. This implies a natural frequency ω range from 5.92·2π to 17.7·2π as assumed in Table 3-1.
2. This implies a damping factor ζ of 0.54 as assumed in Table 3-1.

2.2 Differential Transmitter (TX) Output Specifications

See the Draft Specification for additional notes and a test definition.

Table 2: Summary of Differential Transmitter Output Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{TX-DIFFp-p\_L}$	Differential peak-to-peak output voltage for large voltage swing	900	1300	mV	$V_{TX-DIFFp-p} = 2 * \mid V_{TX-D+} - V_{TX-D-} \mid$ Measured as Note 1
$V_{TX-DIFFp-p\_R}$	Differential peak-to-peak output voltage for regular voltage swing	800		mV	$V_{TX-DIFFp-p} = 2 * \mid V_{TX-D+} - V_{TX-D-} \mid$ Measured as Note 1
$V_{TX-DIFFp-p\_S}$	Differential peak-to-peak output voltage for small voltage swing	520		mV	$V_{TX-DIFFp-p} = 2 * \mid V_{TX-D+} - V_{TX-D-} \mid$ Measured as Note 1
V_{TX-CM_L}	DC common code output voltage for large voltage swing		375	mV	Defined as: $V_{TX-CM} = DC_{(avg)}$ of $\mid V_{TX-D+} + V_{TX-D-} \mid /2$ Measured as: Note 1
V_{TX-CM_S}	DC common mode output voltage for small voltage swing	135	280	mV	Defined as: $V_{TX-CM} = DC_{(avg)}$ of $\mid V_{TX-D+} + V_{TX-D-} \mid /2$ Measured as: Note 1 See also Note 2
$V_{TX-DE-3.5-Ratio}$	De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	-3.0	-4.0	dB	1, 3, 4
$V_{TX-DE-6.0-Ratio}$	De-emphasized differential output voltage ratio for -6 dB de-emphasis	-5.0	-7.0	dB	1, 3, 4
$V_{TX-CM-ACp-p\ L}$	AC peak-to-peak common mode output voltage for large swing		90	mV	$V_{TX-CM-AC} =$ Max $\mid V_{TX-D+} + V_{TX-D-} \mid /2 -$ Min $\mid V_{TX-D+} + V_{TX-D-} \mid /2$ Measured as: Note 1 See also Note 5
$V_{TX-CM-ACp-p\ R}$	AC peak-to-peak common mode output voltage for regular swing		80	mV	$V_{TX-CM-AC} =$ Max $\mid V_{TX-D+} + V_{TX-D-} \mid /2 -$ Min $\mid V_{TX-D+} + V_{TX-D-} \mid /2$ Measured as: Note 1 See also Note 5
$V_{TX-CM-ACp-p\ S}$	AC peak-to-peak common mode output voltage for small swing		70	mV	$V_{TX-CM-AC} =$ Max $\mid V_{TX-D+} + V_{TX-D-} \mid /2 -$ Min $\mid V_{TX-D+} + V_{TX-D-} \mid /2$ Measured as: Note 1 See also Note 5
$V_{TX-IDLE-SE}$	Maximum single-ended voltage in EI condition, DC + AC		50	mV	6, 7
$V_{TX-IDLE-SE-DC}$	Maximum single-ended voltage in EI condition, DC only		20	mV	6, 7, 8
$V_{TX-IDLE-DIFFp-p}$	Maximum peak-to-peak differential voltage in EI condition		40	mV	7
V_{TX-SE}	Single-ended voltage (w.r.t. VSS) on D+/D-	-75	750	mV	1, 9

Table 2: Summary of Differential Transmitter Output Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$T_{TX-Eye-MIN}$	Minimum TX eye width, 3.2 and 4.0 Gb/s	0.7		UI	1, 10
$T_{TX-Eye-MIN-4.8}$	Minimum TX eye width, 4.8 Gb/s	TBD		UI	1, 10
$T_{TX-DJ-DD}$	Maximum TX deterministic jitter, 3.2 and 4.0 Gb/s		0.2	UI	1, 10, 11
$T_{TX-DJ-DD-4.8}$	Maximum TX deterministic jitter, 4.8 Gb/s		TBD	UI	1, 10, 11
$T_{TX-PULSE}$	Instantaneous pulse width	0.85		UI	12
$T_{TX-RISE}$, $T_{TX-FALL}$	Differential TX output rise/fall time	30	90	ps	Given by 20%-80% voltage levels. Measured as: Note 1
$T_{TX-RF-MISMATCH}$	Mismatch between rise and fall times		20	ps	
$RL_{TX-DIFF}$	Differential return loss	8		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note 13
RL_{TX-CM}	Common mode return loss	6		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note 13
R_{TX}	Transmitter termination resistance	41	55	Ω	14
$R_{TX-Match-DC}$	D+/D- TX resistance difference		4	%	$R_{TX-Match-DC} = 2*|R_{TX-D+} - R_{TX-D-}|/(R_{TX-D+} + R_{TX-D-})$ Bounds are applied separately to high and low output voltage states
$L_{TX-SKEW\,1}$	Lane-to-lane skew at TX		100 + 3UI	ps	15, 17
$L_{TX-SKEW\,2}$	Lane-to-lane skew at TX		100 + 2UI	ps	16, 17
$T_{TX-DRIFT-RESYNC}$	Maximum TX Drift (resync mode)		240	ps	18
$T_{TX-DRIFT-RESAMPLE}$	Maximum TX Drift (resample mode only)		120	ps	18
BER	Bit Error Ratio		10^{-12}		19

NOTES:
1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.
2. The transmitter designer should not artificially elevate the common mode in order to meet this specification.
3. This is the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
4. De-emphasis will be disabled in the calibration state.
5. Includes all sources of AC common mode noise.
6. Single-ended voltages below this value that are simultaneously detected on D+ and D- are interpreted as the electrical idle condition.
7. Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output EI specifications.

8. This specification, considered with VRX-IDLE-SE-DC, implies a maximum 15 mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM agents of 26 mV when worst case termination resistance matching is considered.
9. The maximum value is specified to be at least (VTX-DIFFp-p L / 4) + VTX-CM L + (VTX-CM-ACp-p / 2)
10. This number does not include the effects of SSC or reference clock jitter.
11. Defined as the Dual-Dirac deterministic jitter as described in Section 4.
12. Pulse width measured at 0 V differential.
13. One of the components that contribute to the deterioration of the return loss is the ESD structure, which needs to be carefully designed.
14. The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed ± 5 and with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
15. Lane to lane skew at the transmitter pins for an end component.
16. Lane to lane skew at the transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the receiver pins of the incoming PORT).
17. This is a static skew. An FB-DIMM component cannot change its lane to lane phase relationship after initialization.
18. Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
19. BER per differential lane. Refer to Section 4 for a complete definition of Bit Error Ratio.

2.3 Differential Transmitter (TX) Compliance Eye Diagrams

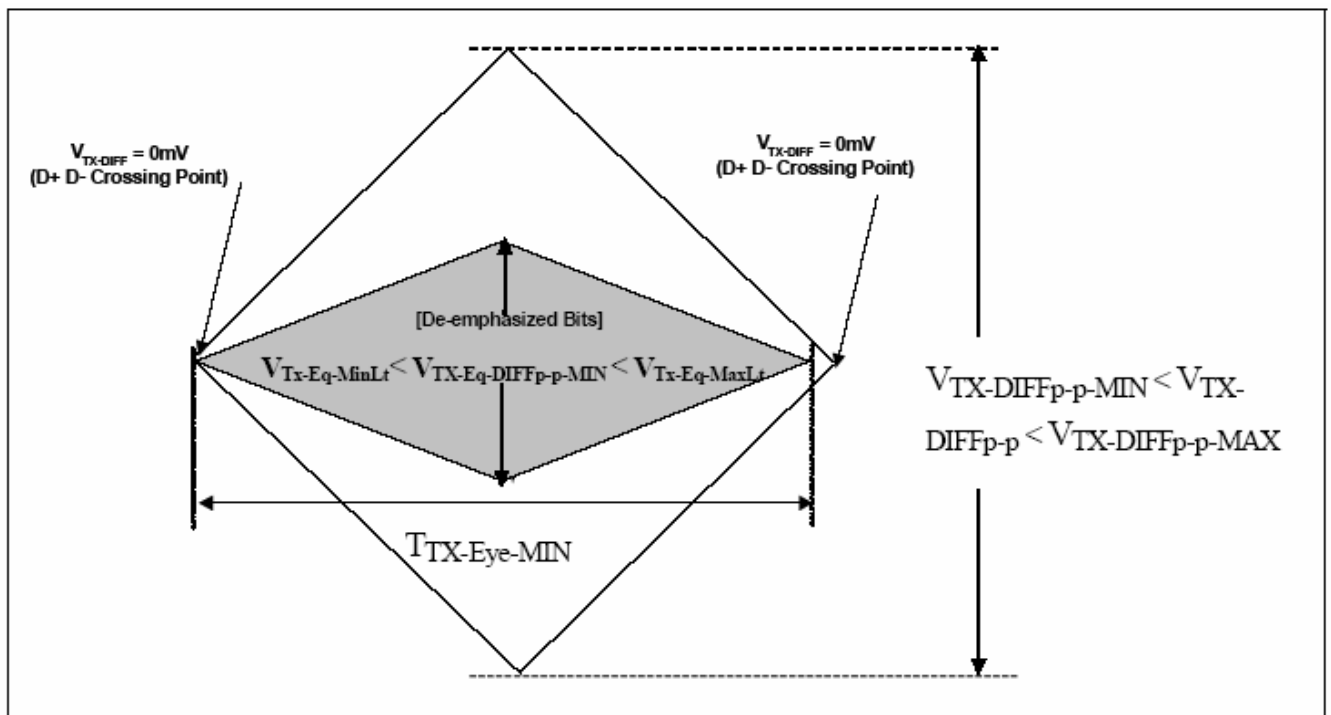Refer Section 3.3.1 of the Draft Specification for eye diagram definition.

Figure 1: Transmitter output eye specifications, with and without de-emphasis

2.4 Differential Receiver (RX) Input Specifications

See the Draft Specification for additional notes and test definitions.

Table 3: Summary of Differential Receiver Input Specification (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	170	1300	mV	$V_{RX-DIFFp-p} = 2^*|V_{RX-D+} - V_{RX-D-}|$ Measured as: Note 1
$V_{RX-IDLE-SE}$	Maximum single-ended voltage for EI condition (AC + DC)		65	mV	2, 3, 4, 5
$V_{RX-IDLE-SE-DC}$	Maximum single-ended voltage for EI condition (DC only)		35	mV	2, 3, 4, 5, 6
$V_{RX-IDLE-DIFFp-p}$	Maximum peak-to-peak differential voltage for EI condition		65	mV	3, 4, 5
V_{RX-SE}	Single-ended voltage (w.r.t. VSS) on D+/D-	-300	900	mV	4
$V_{RX-DIFF-PULSE}$	Single-pulse peak differential input voltage	85		mV	4, 7
$V_{RX-DIFF-ADJ-RATIO-HI}$	Amplitude ratio between adjacent symbols, $1100\ mV < V_{RX-DIFFp-p} <= 1300\ mV$		3.0		4, 8
$V_{RX-DIFF-ADJ-RATIO}$	Amplitude ratio between adjacent symbols, $V_{RX-DIFFp-p} <= 1100\ mV$		4.0		4, 8
$T_{RX-TJ-MAX}$	Maximum RX inherent timing error, 3.2 and 4.0 Gb/s		0.4	UI	4, 9, 10
$T_{RX-TJ-MAX-4.8}$	Maximum RX inherent timing error, 4.8 Gb/s		TBD	UI	4, 9, 10
$T_{RX-DJ-DD}$	Maximum RX inherent deterministic timing error, 3.2 and 4.0 Gb/s		0.3	UI	4, 9, 10, 11
$T_{RX-DJ-DD-4.8}$	Maximum RX inherent deterministic timing error, 4.8 Gb/s		TBD	UI	4, 9, 10, 11
$T_{RX-PW-ZC}$	Single-pulse width at zero-voltage crossing	0.55		UI	4, 7
$T_{RX-PW-ML}$	Single-pulse width at minimum-level crossing	0.2		UI	4, 7
$T_{RX-RISE}, T_{RX-FALL}$	Differential RX input rise/fall time	50		ps	Given by 20%-80% voltage levels.
V_{RX-CM}	Common mode of the input voltage	120	400	mV	Defined as: $V_{RX-CM} = DC_{(avg)}$ of $|V_{RX-D+} + V_{RX-D-}|/2$ Measured as: Note 1 See also Note 12
$V_{RX-CM-ACp-p}$	AC peak-to-peak common mode of input voltage		270	mV	$V_{RX-CM-AC} =$ Max $|V_{RX-D+} + V_{RX-D-}|/2-$ Min $|V_{RX-D+} + V_{RX-D-}|/2$ Measured as: Note 1
$V_{RX-CM-EH-Ratio}$	Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$		45	%	13

Table 3: Summary of Differential Receiver Input Specification (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Comments
$RL_{RX-DIFF}$	Differential return loss	9		dB	Measured over 0.1GHz to 2.4GHz. See also Note 14
RL_{RX-CM}	Common mode return loss	6		dB	Measured over 0.1GHz to 2.4GHz. See Also Note 14
R_{RX}	RX termination resistance	41	55	Ω	15
$R_{RX-Match-DC}$	D+/D- RX resistance difference		4	%	$R_{RX-Match-DC} =$ $2*|R_{RX-D+} - R_{RX-D-}|/(R_{RX-D+} + R_{RX-D-})$
$L_{RX-PCB-SKEW}$	Lane-to-lane PCB skew at Rx		6	UI	Lane-to-lane PCB skew at the receiver that must be tolerated. See also Note 16
$T_{RX-DRIFT}$	Minimum RX Drift Tolerance	400		ps	17
F_{TRK}	Minimum data tracking 3 dB bandwidth	0.2		MHz	18
$T_{EI-ENTRY-DETECT}$	Electrical idle entry detect time		60	ns	19
$T_{EI-EXIT-DETECT}$	Electrical idle exit detect time		30	ns	
BER	Bit Error Ratio		10^{-12}		20

NOTES:
1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- is interpreted as the Electrical Idle condition. Worst case margins are determined by comparing EI levels with common mode levels during normal operation for the case with transmitter using small voltage swing. See Figure 3-16 and Figure 3-17.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4. Specified at the package pins into a timing and voltage compliance test setup.
5. Receiver designers may implement either single-ended or differential EI detection. Receivers must meet the specification that corresponds to the implemented detection circuit.
6. This specification, considered with $V_{TX-IDLE-SE-DC}$, implies a maximum 15 mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM agents of 26 mV when worst case termination resistance matching is considered.
7. See Figure 3-13 and Figure 3-14. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eye mask.
8. See Figure 3-15. The relative amplitude ratio limit between adjacent symbols prevents excessive inter-symbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
9. This number does not include the effects of SSC or reference clock jitter.
10. This number includes setup and hold of the RX sampling flop.
11. Defined as the Dual-Dirac deterministic timing error as described in Section 4.
12. Allows for 15 mV DC offset between transmit and receive devices.
13. The received differential signal must satisfy this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if VRX-DIFFp-p is 200 mV, the maximum AC peak-to-peak common mode is the lesser of (200 mV *0.45 = 90 mV) and VRX-CM-ACp-p.
14. One of the components that contribute to the deterioration of the return loss is the ESD structure that needs to be carefully designed.

15. The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed ± 5 Ω with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
16. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.
17. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
18. This bandwidth number assumes that the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI, see Section 4 for full jitter tolerance mask.
19. The specified time includes the time required to forward the EI entry condition.
20. BER per differential lane. Refer to Section 4 for a complete definition of Bit Error Ratio.

2.5 Receiver Compliance Eye Diagrams

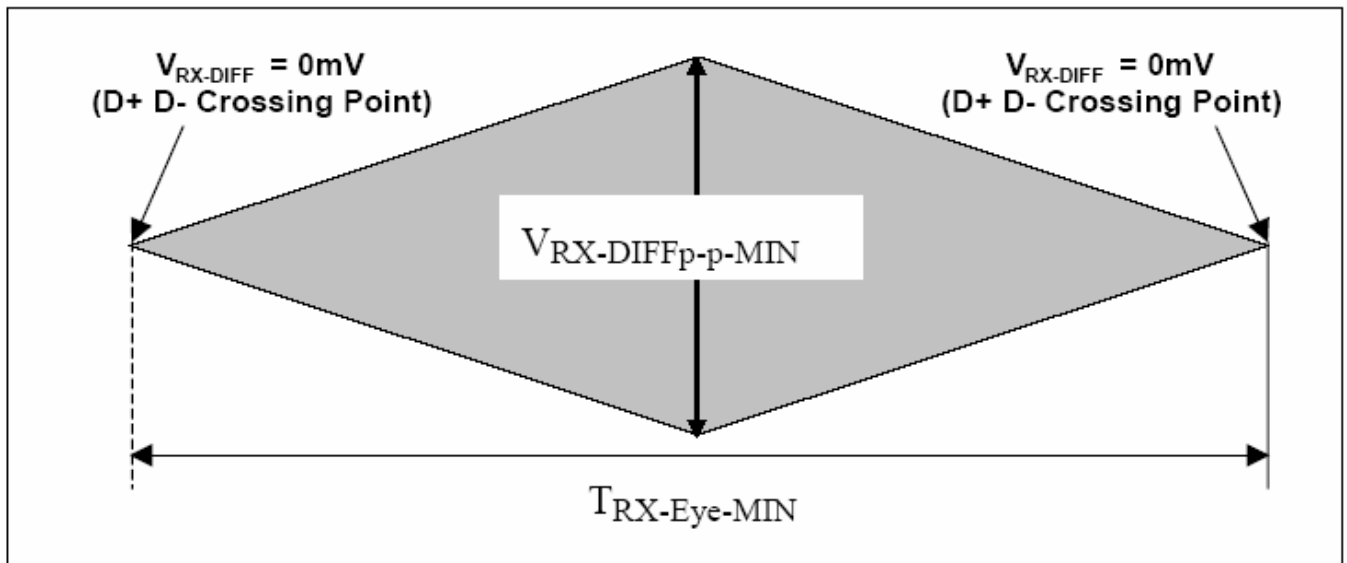See Section 3.4.1 of the Draft Specification for eye diagram definition.

Figure 2: Receiver input eye voltage and timing specifications

2.6 Reference Clock Specifications

See the Draft Specification for additional notes and test definitions.

Table 4: Summary of Reference Clock Input Specifications (Sheet 1of 2)

Symbol	Parameter	Min	Max	Units	Notes
$f_{Refclk-3.2}$	Reference clock frequency @ 3.2 Gb/s (nominal 133.33 MHz)	126.67	133.40	MHz	1, 2, 3
$f_{Refclk-4.0}$	Reference clock frequency @ 4.0 Gb/s (nominal 166.67 MHz)	158.33	166.75	MHz	1, 2, 3
$f_{Refclk-4.8}$	Reference clock frequency @ 4.8 Gb/s (nominal 200 MHz)	190.00	200.10	MHz	1, 2, 3
V_{max}	Single-ended maximum voltage		1.15	V	4, 6
V_{min}	Single-ended minimum voltage	-0.3		V	4, 7
$V_{Refclk-diff-ih}$	Differential voltage high	150		mV	5
$V_{Refclk-diff-il}$	Differential voltage low		-150	mV	5
V_{Cross}	Absolute crossing point	250	550	mV	4, 8, 9
$V_{Cross-delta}$	V_{Cross} variation		140	mV	4, 8, 10
$V_{Refclk-cm-acp-p}$	AC common mode		225	mV	11
$ER_{Refclk-diffRrise,}$ $ER_{Refclk-diff-Fall}$	Rising and falling edge rates	0.6	4.0	V/ns	5, 12
$ER_{Refclk--Match}$	% mismatch between rise and fall edge rates		20	%	4, 13
$T_{Refclk-Dutycycle}$	Duty cycle of reference clock	40	60	%	5
$V_{RB-diff}$	Ringback voltage threshold	-100	100	mV	5, 14
T_{Stable}	Allowed time before ringback	500		ps	5, 14
I_{I_CK}	Clock leakage current	-10	10	μA	15, 16
C_{I_CK}	Clock input capacitance	0.5	2.0	pF	16
$C_{I\_CK(\Delta)}$	Clock input capacitance delta	-0.25	0.25	pF	Difference between RefClk and RefClk# input capacitance

Table 4: Summary of Reference Clock Input Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
ω_1	Natural frequency PLL1	$5.92 \cdot 2\pi$		Mrad/s	17, 18
ζ_1	Damping factor PLL1	0.54			17, 18
ω_2	Natural frequency PLL2		$17.7 \cdot 2\pi$	Mrad/s	17, 19
ζ_2	Damping factor PLL2	0.54			17, 19
T1	Transport delay		5	ns	17, 20
ω_3	Data tracking bandwidth	$200 \cdot 2\pi$		krad/s	17, 21
N_{SAMPLE}		10^{12}		periods	22
$T_{REF\text{-}JITTER\text{-}RMS}$	Reference clock jitter (rms), filtered		3.0	ps	23, 24
$T_{REF\text{-}JITTER\text{-}DELTA}$	Reference clock jitter difference between adjacent AMBs		TBD	ps	

NOTES:

1. The nominal reference clock frequency is determined by the data frequency of the link divided by 2 times the fixed PLL multiplication factor for the FB-DIMM channel (6:1). f_{data} = 2000 MHz for a 4.0 Gbps FB-DIMM channel and so on.
2. Measured with SSC disabled. Enabling SSC will reduce the reference clock frequency as described in Section 3.1.2.
3. Not all FB-DIMM agents will support all frequencies; compliance to the frequency specifications is only required for those data rates that are supported by the device under test.
4. Measurement taken from single-ended waveform.
5. Measurement taken from differential waveform.
6. Defined as the maximum instantaneous voltage including overshoot. See Figure 3-3.
7. Defined as the minimum instantaneous voltage including undershoot See Figure 3-3.
8. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 3-3.
9. Refers to the total variation from the lowest crossing pint to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 3-3.
10. Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in for any particular system. See Figure 3-4.
11. The majority of the reference clock AC common mode occurs at high frequency (that is the reference clock frequency).
12. Measured from -150 mV to + 150 mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential 0 V crossing. See Figure 3-5.
13. Edge rate matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ± 75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median crosspoint is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations. The rising edge rate of REFCLK+ should be compared to the falling edge rate of REFCLK-. The maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 3-6.
14. See Figure 3-7. Tstable is the time the differential clock must maintain a minimum ± 150 mV differential voltage after rising / falling edges before it is allowed to drop back into the ± 100 mV differential range.
15. Measured with a single-ended input voltage of 1 V.

16. Applies to RefClk and RefClk#.
17. This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter TREF-JITTER. This number is valid for 3.2 Gb/s and 4.0 Gb/s operation.
18. Implies a -3 dB bandwidth of 11 MHz and jitter peaking of 3 dB.
19. Implies a -3 dB bandwidth of 33 MHz and jitter peaking of 3 dB.
20. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. See Figure 3-8. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions. This bandwidth number assumes the specified minimum data transition density.
21. Direct measurement of phase jitter records over NSAMPLE periods may be impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at NSAMPLE samples extrapolated from an estimate of the sigma of the random jitter components. For details on this measurement, refer to Section 4.
22. Measured with SSC enabled on reference clock generator.
23. As "measured" after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRX-Total-MIN parameters.

3 Preparing to Take Measurements

3.1 Required Equipment

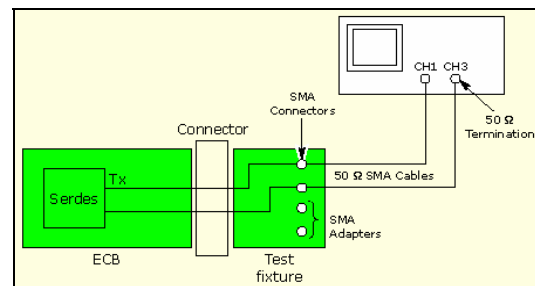The following equipment is required to take measurements:

- TDS6604B or **TDS6804B** or TDS7704B or **TDS6124C** or **TDS6154C** oscilloscope with the RT-Eye software (Opt. RTE- version 2.0) and FB-DIMM Compliance Module (FBD) installed.

- Probes – probing configuration is MOI specific. Refer to each MOI for correct probe configuration.

- Test fixture −Tektronix differential probing fixture- **NEX-TDSFBDP**. To order, click http://www.busboards.com/products/scopeAccessories/tdsfbdp/index.html.

3.2 Probing Options for Transmitter testing

The first step is to probe the link. Currently, the FB-DIMM specifications have defined the ball of the AMB as the test point.
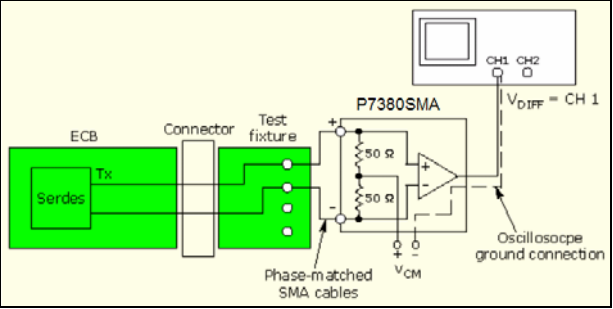
3.2.1 SMA Connection

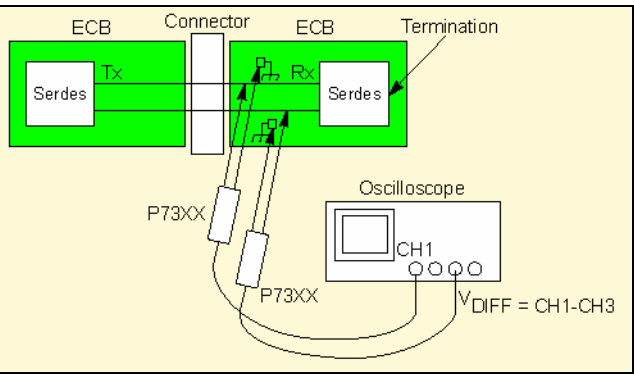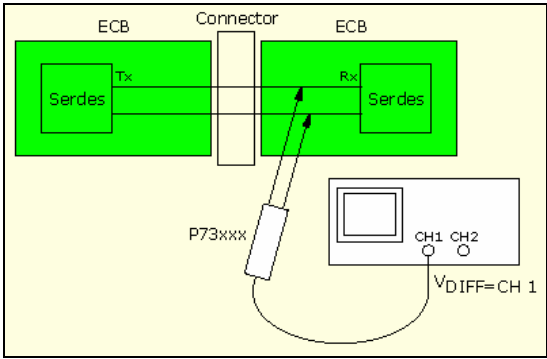| 1. **Two TCA-SMA inputs using SMA cables (Ch1) and (Ch3)** The differential signal is created by the RT-Eye software from the math waveform Ch1-Ch3. The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique requires breaking the link and terminating into a 50 Ω/side termination of the oscilloscope. While in this mode, the FB-DIMM Serdes will transmit the compliance test pattern (IBIST Pattern) to maximize data dependent jitter. Ch-Ch de-skew is required as two channels are used. This configuration does not compensate for cable loss in the SMA cables. The measurement reference plane is at the input of the TCA-SMA connectors on the oscilloscope. Any cable loss should be measured and entered into the vertical attenuation menu for accurate measurements at the SMA Cable attachment point.	 **Probe Configuration A** SMA Psuedo-differential

2. **One P7380SMA differential active probe (Ch1). (Only useful for 3.2 Gb/s data rate)** The differential signal is measured across the termination resistors inside the P7380SMA probe. This probing technique requires breaking the link. While in this mode, the FB-DIMM Serdes will transmit the compliance test pattern to maximize data dependent jitter. Matched cables are provided with the P7380 probe to avoid introducing de-skew into the system. Only one channel of the oscilloscope is used. The P7380SMA provides a calibrated system at the Test Fixture attachment point, eliminating the need of compensating for cable loss associated with the probe configuration A.	**Probe Configuration B** SMA Input Differential Probe

3.2.2 AMB Ball connection

3. **Two active probes (Ch1) and (Ch3)** The differential signal is created by the RT-Eye software from the math waveform Ch1-Ch3. The Common mode AC measurement is also available in this configuration from the common mode waveform (Ch1+Ch3)/2. This probing technique can be used for either a live link that is transmitting data, or a link that is terminated into a "dummy load." In both the cases, the single-ended signals should be probed as close as possible to the termination resistors on both sides with the shortest ground connection possible. Ch-Ch de-skew is required because two channels are used.	**Probe Configuration C** Two Single-ended Active Probes

4. **One P7380 (3.2 Gb/s data rate only)/P7313 Differential probe (Ch1)**
   The differential signal is measured directly across the termination resistors. This probing technique can be used for either a live link that is transmitting data, or a link terminated into a "dummy load." In both cases, the signals should be probed as close as possible to the termination resistors. De-skew is not necessary as a single channel is used.

Probe Configuration D

One Differential Active Probe

3.3 Initial Oscilloscope Setup

After connecting the Device Under Test (DUT), follow the proper probing configuration for the test. Click the DEFAULT setup button and the AUTOSET to display the serial data bit stream.

3.4 Running the RT-Eye Software

1. Go to **File> Run Application> RT-Eye Serial Compliance and Analysis**. For B and C series oscilloscopes, select **App>RT-Eye** …. Please refer to the OLH.
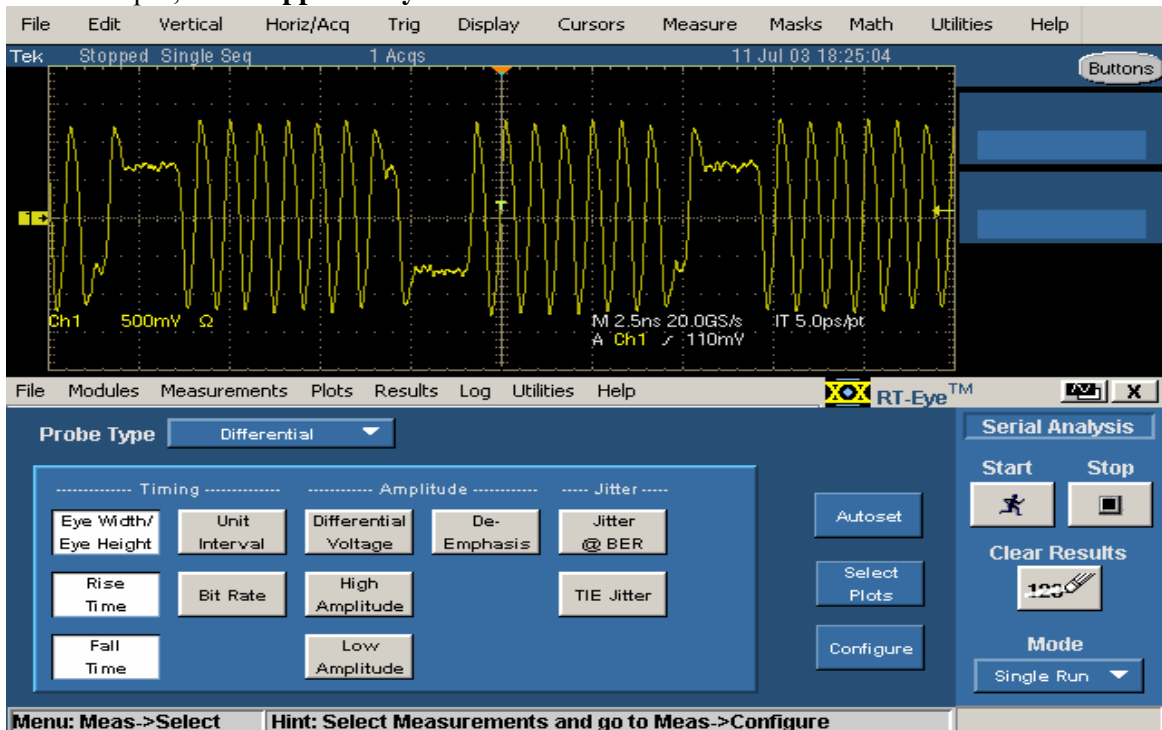

Figure 3: Default menu of the RT-Eye software

Figure 3 shows the oscilloscope display. The default mode of the software is the **Serial Analysis** module (Opt. RTE-Version 2.0). This software is intended for generalized Serial Data analysis on 8B/10B encoded copper links.

2. Select the FB-DIMM Compliance Module from the **Modules** pull-down list.

Figure 4: Choosing FB-DIMM Compliance Module

Note: If FB-DIMM does not appear in the list, the FB-DIMM Compliance Module (Opt. FBD) has not been installed.

The rest of this MOI document details use of the FB-DIMM Compliance Module to perform electrical compliance measurements.

For additional information about the FB-DIMM Compliance Module, refer to the online help, which is available in the Help Menu for the RT-Eye software.

3.5 Clock Recovery

Second-order PLL is used. Refer to section 2.X of Common Specifications between TX and RX in the Draft Specifications. Also refer to Table 1 of this MOI. (Serial analysis has several CDRs. You can configure the CDR in the SA module to be exactly the same as that in FB-DIMM.)

4 FB-DIMM Receiver (RX) Compliance Testing

This section provides the Methods of Implementation (MOIs) for Receiver tests using a Tektronix real-time oscilloscope, probes, the RT-Eye compliance software solution (version 2.0), and with the Tektronix test fixture - NEX-TDSFBDP / JEDEC parametric test fixture.

To order FBD scope probe kit, click
http://www.busboards.com/products/scopeAccessories/tdsfbdp/index.html

4.1 Probing the Link for RX Compliance

Use probing configuration (B or D) to probe the link differentially at a point close to the pins of the receiver device.

This method (using the Tektronix NEX-TDSFBDP FBD scope probe kit and P7313 probes) of probing at the ball of the RX AMB:
- Is the only direct method of testing the eye opening at the receiver.
- Includes all segments of the transmission channel: TX board loss, Connector Loss (both TX and RX side), and RX board loss.

- Both Common Mode and Differential Mode measurements can be made directly. This method indirectly assures Slot Connector Compliance if a compliant standard blank DIMM Module is used as the test vehicle.

- The **NEX-TDSFBDP** test fixtures provide the flexibility to perform Differential and Common Mode measurements. This test fixture consists of four blank DIMMs with ten probe tip clip connectors and termination resistors. The user can solder up to three probe tip clip connectors to the relevant South Bound Receiver lanes on one blank DIMM and test a maximum of three FB-DIMM South Bound lines. The user can also configure the NEX-TDSFBDP test fixture to test the remaining seven South Bound lanes or Reference Clock.
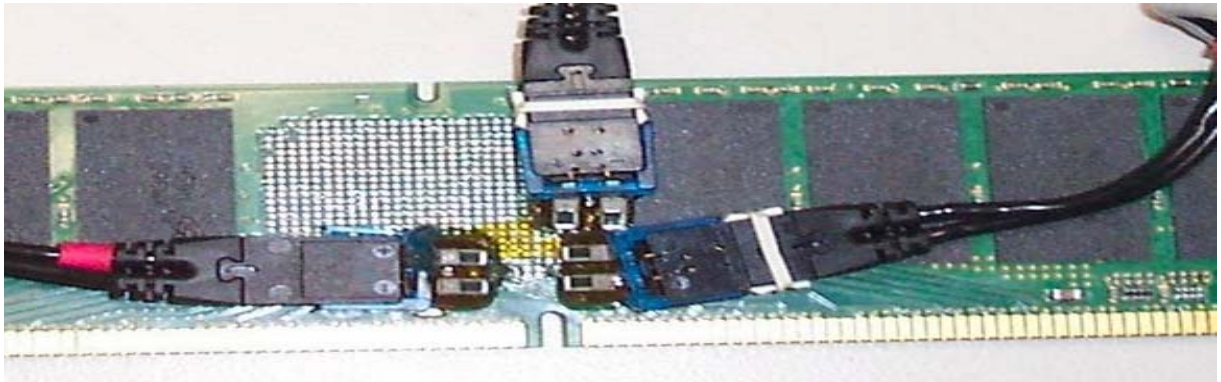

Figure 5: NEX-TDSFBDP test fixture

Alternatively, use probing configuration A or C using Ch1 and Ch3 inputs of an oscilloscope (using an SMA break out fixture) that has 40 GS/s sample rate available on two channels (only TDS6124C and TDS6154C series).

4.2 Running a Complete RX Compliance Test

The MOIs for each RX test are documented in the following sections. All RX measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all receiver measurements:

1. In the FBDIMM module, set the Bit Rate to 3.2 Gb/s, 4.0 Gb/s or 4.8 Gb/s.

2. Select **Receiver** from the Test Point pull-down list.

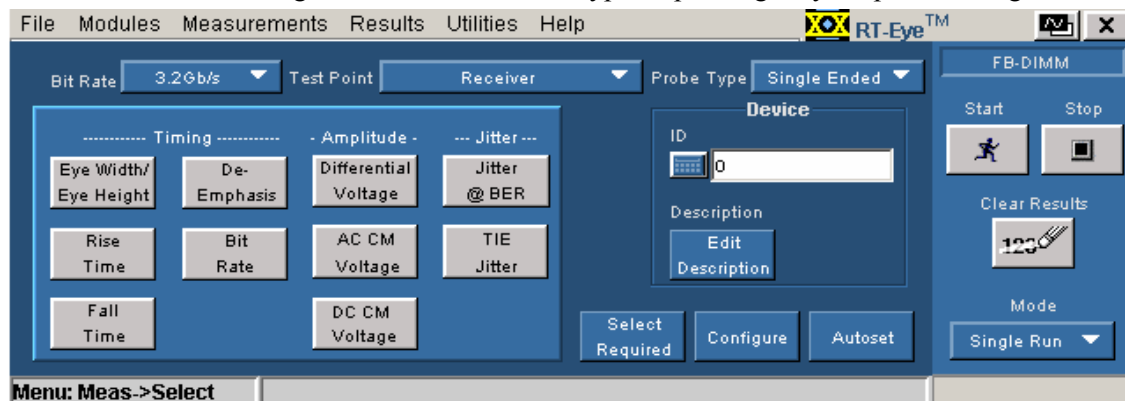3. Select Differential or Single-Ended as the Probe Type, depending on your probe configuration.

Figure 6: Measurements select menu setup

4. Click **Select Required**.

5. Click **Configure** to access the Configuration menus and to set up Signal Source.

6. Click Autoset to auto set signal and reference levels.

7. Click **Start** and choose between single run or continue run.

Figure 7 shows the result of a Receiver Compliance test on a signal that passes all receiver tests.
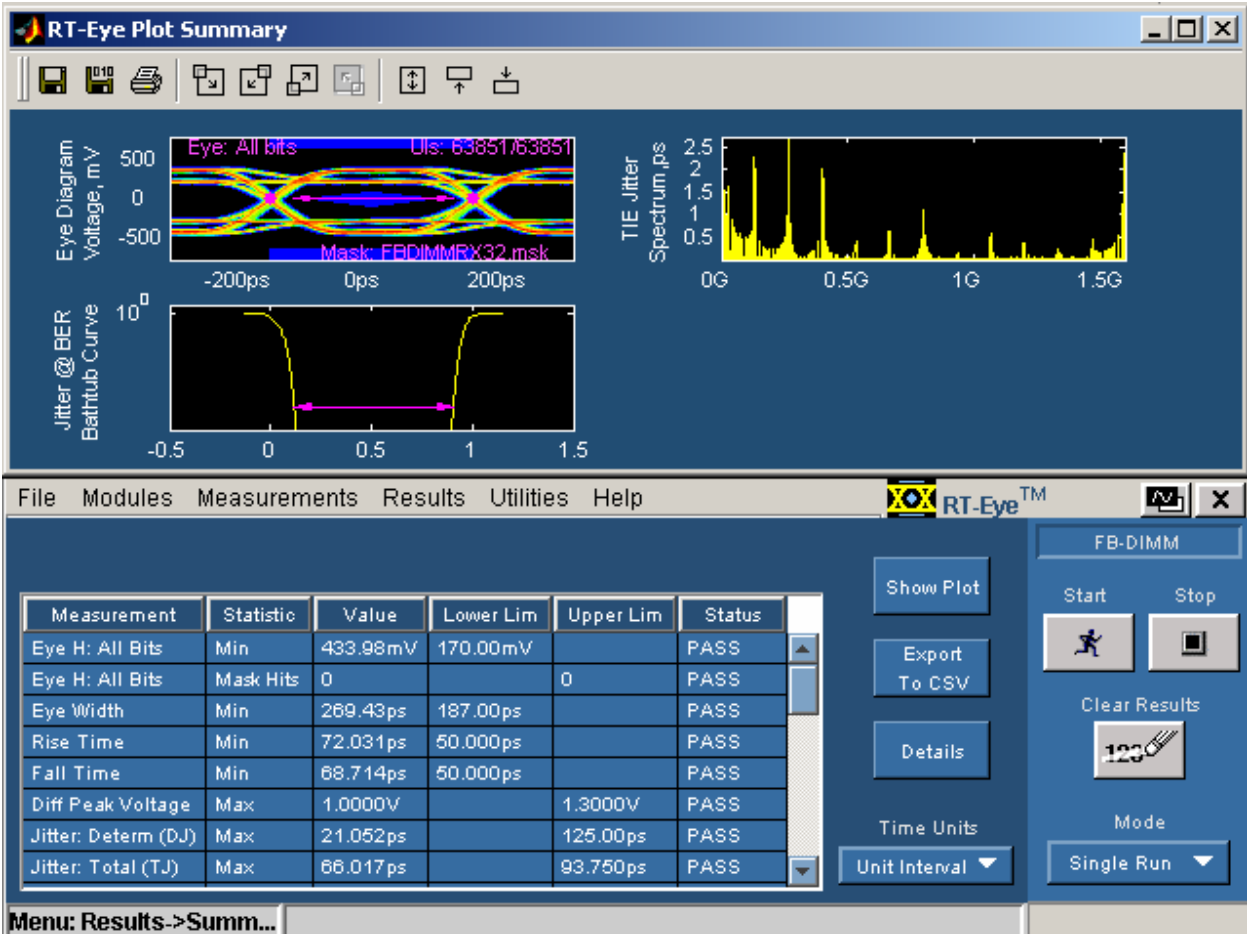
Figure 7: Result of completed receiver compliance test

4.2.1 RX Differential Pk-Pk Input Voltage MOI

Test Definition Notes from the Specification:

- $V_{RX-DIFFp-p} = 2*|V_{RX-D+} - V_{RX-D-}|$

- Specified at the measurement point and measured over the entire data. The test load in Figure 1-1 (Draft Specification) should be used as the RX device while taking measurements. Also refer to the receiver compliance eye diagram shown in Figure 3-12 (Draft Specification).

$V_{RX-DIFFp-p}$ (Differential Input Pk-Pk Voltage) is defined in Table 3-12 (Draft Specification). Differential Pk-Pk Voltage characteristics are: Maximum = 1.3 V and Minimum = 0.170 V. This

measurement is solved by two measurements: Differential Peak Voltage and Eye Height measurement.

Test Procedure:

Follow the procedure in Section 5.3.1 (of this MOI), ensuring that **Differential Voltage** is selected in the **Measurements> Select** menu.

PASS Condition:

$V_{RX-DIFFp-p}$ < 1.3 V and 170 mV < Eye Height

Measurement Algorithm:

Refer to section 5.3.1 of this MOI document for Differential Voltage measurement and Eye Height measurement algorithms.

Note: For receiver testing, Eye Height is measured on all UIs. There is no separate Eye Height for Transition bits measurement and Non-Transition bits measurement.

4.2.2 Minimum RX Eye Width MOI

Test Definition Notes from the Draft Specification:

- The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = .6UI$. T_RX-TJ_MAX in Table 3-4 is 0.4 UI for 3.2 and 4.0 Gb/s. You can derive from it to get T_RX-EYE.

- Specified at the measurement point and measured over the entire data. The test load in Figure 1-1 (Draft Specification) should be used as the RX device while taking measurements. Also refer to the receiver compliance eye diagram shown in Figure 3-12 (Draft Specification).

- A TJ = 0.4 UI provides for a total sum of deterministic and random jitter budget for the transmitter and interconnect. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.4 UI jitter budget collected over the entire data.

Note: The median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. T_{RX-EYE} (Minimum RX Eye Width) is defined in Table 4-6 of Version 1.0a of the Draft Specification.

Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **Eye Width/Eye Height** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

Refer to section 3.4.1 and 4.8 of the Draft Specification for Eye Width measurement algorithm.

4.2.3 RX AC Common Mode Input Voltage MOI

Test Definition Notes from Specification:

$$VRX - CM - AC = \frac{Max|VRX\text{-}D++VRX\text{-}D\text{-}|}{2} - \frac{Min|VRX-D++VRX-D-|}{2}$$

- Specified at the measurement point and measured over entire data. The test load in Figure 1-1 (Draft Specification) should be used as the RX device when taking measurements. Also refer to the receiver compliance eye diagram shown in Figure 3-12 (Draft Specification). $V_{RX-CM-ACp}$ (AC Peak Common Mode Input Voltage) is defined in Table 3-4 (Draft Specification).

Limits:

Maximum = 270 mV and the pass condition is 270 mV > $V_{RX-CM-ACp}$

Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **AC CM Voltage** is selected in the **Measurements> Select** menu.

Note: AC CM voltage is available only when you select Single-ended probe type.

Measurement Algorithms:

This measurement is made over the entire data defined in Section 3.4 (Draft Specification).

AC CM Pk Voltage Measurement:

The AC Common Mode Pk Voltage measurement returns the peak-to-peak value of common mode. (Peak-to-peak value is not affected by DC).

4.2.4 RX DC Common Mode Input Voltage MOI

Test Definition Notes from the Specification:

$$VRX - CM = DC(avg)of \frac{|VRX\text{-}D++VRX\text{-}D\text{-}|}{2}$$

- Specified at the package pins into a timing and voltage compliant test load. Note that the signal levels at the pad will be lower than at the pin.

Limits:

Maximum = 400mV and Minimum = 120mV

Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **DC CM Voltage** is selected in the **Measurements> Select** menu (Note: DC CM Voltage is only available when you select Single-Ended probe type.)

Measurement Algorithms:

This measurement is made over the entire data defined in Section 3.4 (Draft Specification).

The DC Common Mode measurement:

The DC Common Mode measurement returns the DC Average of the Common Mode Voltage waveform.

4.2.5 RX Waveform Eye Diagram Mask Test MOI

Test Definition Notes from the Specification:

- The RX eye diagram in Figure 3-12 (Draft Specification) is specified using the passive compliance/test measurement load (see Figure 1-1, Draft Specification) in place of any real FB-DIMM RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 1-1, Draft Specification) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input receiver of any real FB-DIMM component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics, which cause the real FB-DIMM component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. The RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 3-12, Draft Specification) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon.

- The RX Eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

- The Eye diagram must be valid for the entire data.

 Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **Eye Width /Eye Height** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

This measurement is made over the entire data defined in Section 3.4 (Draft Specification).

The acquisition points are compared to the mask geometry (defined in Figure 4.24, Draft Specification) and mask collisions are reported as Mask Hits in the Measurement Results area.

If Mask Hits > 0, then a failure is indicated in the Measurement Results table.

4.2.6   RX Input Rise/Fall Time test MOI

Test Definition Notes from the Specification:

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 1.1 (Draft Specification) and measured over the entire data. Also refer to the Receiver compliance (Draft Specification).

- Measured between 20-80% at Receiver pins into a test load as shown in Figure 1.1 (Draft Specification) for both V_{RX-D+} and V_{RX-D-}

$T_{RX-RISE}$, $T_{RX-FALL}$ (D+/D- RX output Rise/Fall Time) is defined in Table 3-3 (Draft Specification).

Limits (specified only at Receiver pins compliance point):

Minimum = 50ps.

Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **Rise Time** and **Fall Time** are selected in the **Measurements> Select** menu.

Measurement Algorithm:

This measurement is made over the entire duration of RX test pattern defined in Section 4 (Draft Specification).

Rise/Fall time is limited to rising or falling edges of consecutive transitions for transmitter measurements. (Even for single-ended, the differential waveform is computed and then the rise/fall measurement performed.)

Note: Change the following descriptions to differential waveform only.

Rise Time: The Rise Time measurement is the time difference between when the $V_{REF\text{-}HI}$ reference level is crossed and the $V_{REF\text{-}LO}$ reference level is crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

t_{RISE} is a Rise Time measurement

t_{HI+} is a set of t_{HI} only for rising edges

t_{LO+} is a set of t_{LO} only for rising edges

i and j are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+}

n is a the index of rising edges in the waveform

Fall Time: The Fall Time measurement is the time difference between when the $V_{REF\text{-}HI}$ reference level is crossed and the $V_{REF\text{-}LO}$ reference level is crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

t_{FALL} is a Fall Time measurement

t_{HI-} is set of t_{HI} only for falling edge

t_{LO-} is set of t_{LO} only for falling edge

i and j are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n-is the index to falling edges in the waveform

4.2.7 RX Tj Test MOI

Test Definition Notes from the Specification:

Maximum receiver inherent timing error (Jitter)

Specified at the package pins into a timing and voltage compliance test load.

This value does not include the effects of SSC or ref clk jitter.

This includes the setup and hold of receiving sampling clock.

Limits:

Maximum = 0.4 UI for 3.2 and 4.0 Gb/s data rate.

Maximum = **TBD** UI for 4.8 Gb/s data rate.

Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **Jitter@BER** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

Total jitter is usually comprised of both random and deterministic components. In general, the DJ component has its own PDF (Probability Distribution function), and the combined total jitter PDF is a convolution of the DJ and RJ PDF's. The Rx-Tj is estimated by equivalently deriving the CDF (Cumulative Distribution Function) at measured points and extrapolating to a BER < 10^{-9}, such that a device exceeding the TJ specification is identified with a 99.7% confidence interval.

4.2.8 RX Dj Test MOI (Using Dual-Dirac Method)

Test Definition Notes from the Specification:

-This is the Maximum inherent deterministic timing error (Jitter) specified at the package pins into a timing and voltage compliance test load.

-This value does not include the effects of SSC or ref clk jitter.

-This includes the setup and hold of receiving sampling clock.

-Defined as the Dual-Dirac timing error.

Limits:

Maximum = 0.3 UI for 3.2 and 4.0 Gb/s data rate.

Maximum = **TBD** for 4.8 Gb/s data rate.

Test Procedure:

Follow the procedure in Section 4.3 (Draft Specification), ensuring that **Jitter@BER** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

The DJ PDF is defined as a pair of Dirac delta functions (Dual-Dirac). The Dual-Dirac model is assumed for system. The Dual-Dirac description is merely the linearization of the CDF (Cumulative Distribution Function) at a particular BER. Since the CDF has two sides, this linearization is performed twice, and the result is then combined. The Rx-Dj is estimated by equivalently deriving the CDF at measured points and extrapolating to a BER $< 10^{-9}$, such that a device exceeding the DJ specification is identified with a 99.7% confidence interval.

5 FB-DIMM Transmitter (TX) Compliance Testing

This section provides the Methods of Implementation (MOIs) for Transmitter tests using a Tektronix real-time oscilloscope, probes, and the RT-Eye compliance software with FB-DIMM (FBD) Module.

5.1 Probing the Link for TX Compliance

Use probing configuration (B or D) to probe the link differentially at a point close to the pins of the receiver device.

Alternatively, use probing configuration (A or C) using the Ch1 and Ch3 inputs of an oscilloscope that has a 40 GS/s sample rate available on two channels along with an SMA break-out fixture (TDS6124C and TDS6154C Series).

Since probing at the ball of the TX AMB is not practical, you can use an SMA break-out fixture or a JEDEC approved parametric fixture to test the TX points. However use care about the following when you use an SMA break-out fixture or a JEDEC approved parametric fixture:

- Compensation of all the losses: a.) Transmission channel; TX board loss, b.) Connector Loss (both TX and RX side), and c.) RX board losses are taken into consideration.
- Pseudo-differential measurements should be performed carefully and channel deskew plays an important role.

5.1.1 TX Compliance Test Load

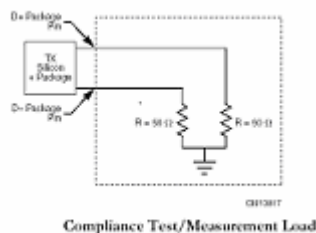The compliance test load for Transmitter compliance is shown in Figure 8.

Compliance Test/Measurement Load

Figure 8: Transmitter Compliance Test Load

5.2 Running a TX Compliance Test

The only test point defined in the FB-DIMM specifications, for the TX Compliance Test is the TX pins on the ball of the AMB. You can use the **SMA** break-out test fixture or the JEDEC test fixture (measures at the connector and not at the ball of the AMB) if it is available. Care should be taken to ensure that the test fixture does not add losses to the FB-DIMM signals. The test point that will be defined by the transmitter test in the FB-DIMM Compliance Module is defined at installation of Version 2.0 of the RT-Eye software. Version 2.0 supports only the Transmitter Pins Compliance point. Refer to section 3.2 for more information on installing the proper test point. The transmitter data rates can be 3.2 GB/s, 4.0 Gb/s, or 4.8 Gb/s. Each of these rates can have three voltage swing settings and in each voltage swing setting you can have three de-emphasis levels. The following table provides the details:

Table 5: Transmitter test point details

Specification Select	Rate Select	Test Point Select	Swing	De-Emphasis
Rev 0.7 May 10, 2005	3.2Gb/s	Transmitter	Large	No De-Emphasis
				-3.5dB
				-6.0dB
			Regular	No De-Emphasis
				-3.5dB
				-6.0dB
			Small	No de-Emphasis
				-3.5dB
				-6.0dB
Rev 0.7 May 10, 2005	4.0Gb/s	Transmitter	Large	No De-Emphasis
				-3.5dB
				-6.0dB
			Regular	No De-Emphasis
				-3.5dB
				-6.0dB
			Small	No De-Emphasis
				-3.5dB
				-6.0dB
Rev 0.7 May 10, 2005	4.8Gb/s	Transmitter	Large	No De-Emphasis
				-3.5dB
				-6.0dB
			Regular	No De-Emphasis
				-3.5dB
				-6.0dB
			Small	No De-Emphasis
				-3.5dB
				-6.0dB

The MOI for each of the Transmitter tests is documented in the following sections. All Transmitter measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all transmitter measurements:

1. In the **Measurements> Select** menu (Figure 9), select **Bit rate** (3.2/4.0/4.8Gb/s).

2. Click **Transmitter** from the **Test Point** pull-down list.

3. Select **Single-Ended** (probe configurations A & C defined in Section 3) or **Differential** (Probe configurations B & D defined in Section 3) as the **Probe Type,** depending on your probe configuration.

4. Click **Configure** to access the Configuration menus and set up the Signal Source. Click Select to return to the **Measurements> Select** menu.
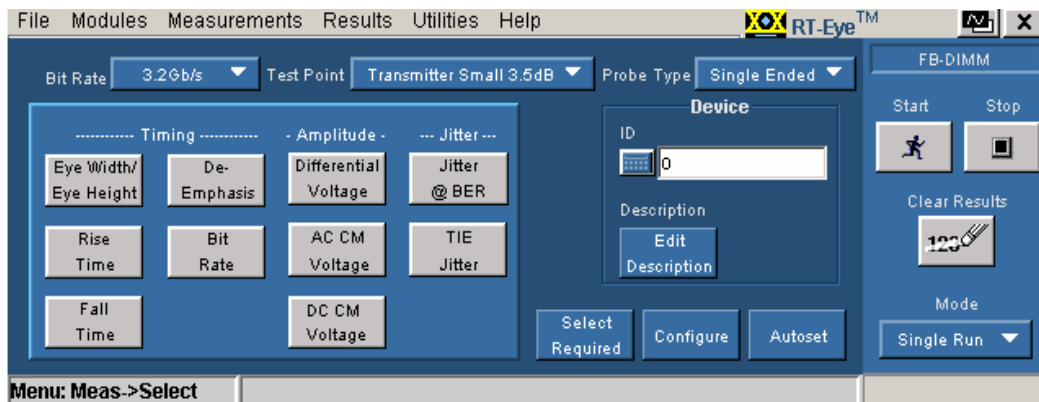

Figure 9: Measurements select menu setup

5. Click the desired measurements or click **Select Required**.

6. Click **Autoset** to auto set signal and reference levels.

7. Click **Start**.

Figure 10 shows the result of a Transmitter Compliance test on a signal that passes the transmitter tests at TX compliance test points.
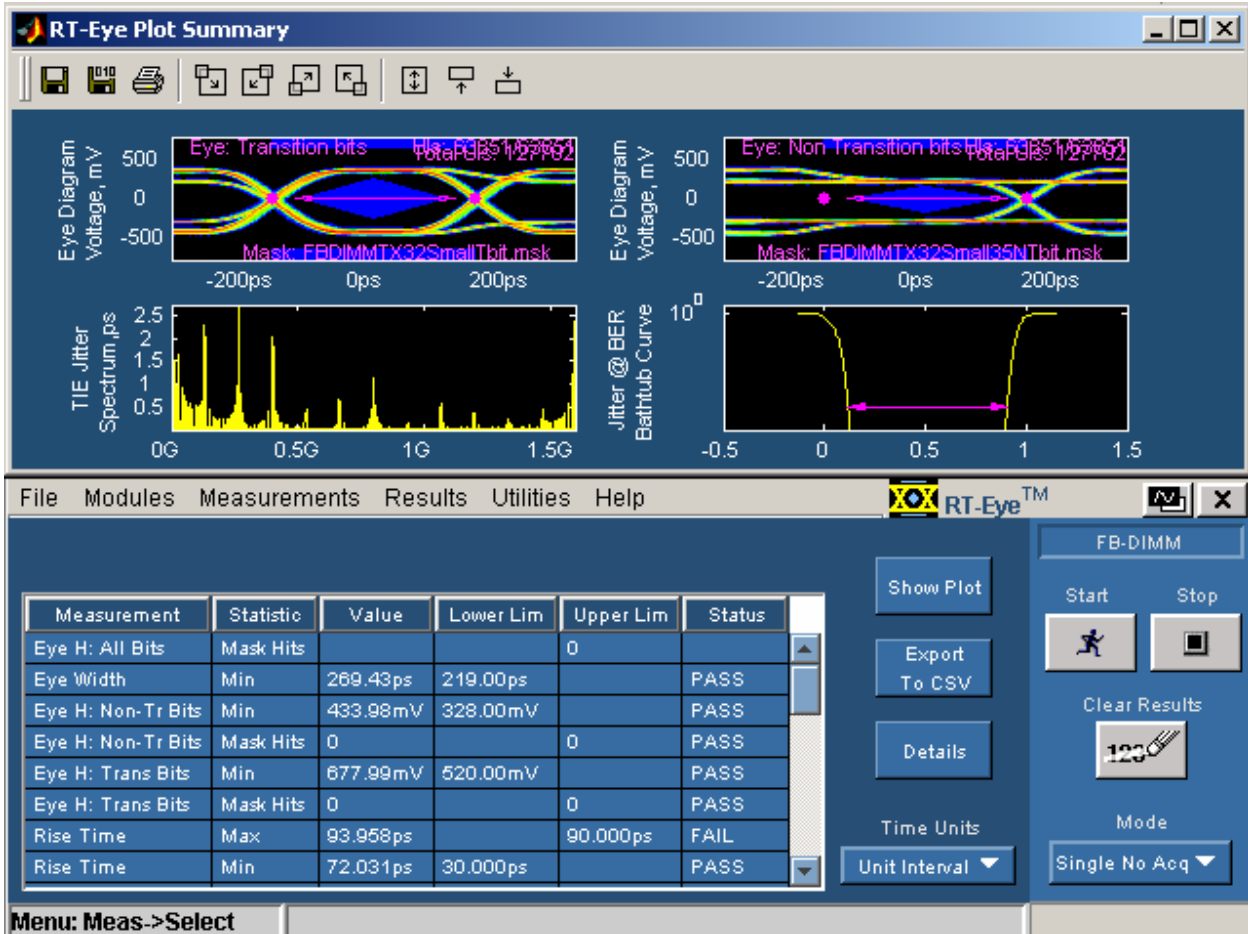
Figure 10: Result of a completed compliance test at the transmitter pins

5.2.1 TX Differential Pk-Pk Output Voltage MOI

Test Definition Notes from the Specification:

- $V_{TX-DIFFp-p} = 2*|V_{TX-D+} - V_{TX-D-}|$

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 1-1 (Draft Specification) and measured over entire TX test pattern as specified in section 4 of the draft specification. Also refer to the transmitter compliance eye diagram shown in Figure 3-9 (Draft Specification).

$V_{TX-DIFFp-p}$ (Differential Output Pk-Pk Voltage) is defined in Table 3-3 (Draft Specification). Differential Pk-Pk Voltage characteristics are:

Maximum = 1.3 V and

Minimum = 0.90 V (large swing)

or

Minimum = 0.80V (medium swing)

or

Minimum = 0.520V (small swing).

This measurement is solved by two measurements - Differential Peak Voltage measurement and Eye Height: Transition bits measurement. Select Differential Voltage and Eye Width/Eye Height, to get five measurements: Eye Height, Eye Height: Transition bits, Eye Height: Non-Transition bits, Eye Width and Differential Peak Voltage.

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **Differential Voltage** and Eye Width/Eye Height are selected in the **Measurements> Select** menu.

Pass Condition:

Transmitter Pins Compliance Test Point:

Large Voltage Swing:

Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.900 V < Eye Height (No de-emphasis)

Non-Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.567 V < Eye Height (-3.5 dB de-emphasis)

Non-Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.402 V < Eye Height (-6.0 dB de-emphasis)

Regular Voltage Swing:

Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V (Not in the table 3-3 in spec) and 0.800 V < Eye Height (No de-emphasis)

Non-Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.504 V < Eye Height (-3.5 dB de-emphasis)

Non-Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.357 V < Eye Height (-6.0 dB de-emphasis)

Small Voltage Swing:

Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.520 V < Eye Height (No de-emphasis)

Non-Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.328 V < Eye Height (-3.5 dB de-emphasis)

Non-Transition Bit: $V_{TX-DIFFp-p}$ < 1.3 V and 0.232 V < Eye Height (-6.0 dB de-emphasis)

Measurement Algorithm:

These measurements are made over the entire TX test pattern defined in Section 4 (Draft Specification).

Differential Peak Voltage Measurement: The Differential Peak Voltage measurement returns two times the larger of the Min or Max statistic of the differential voltage waveform.

Where:

i is the index of all waveform values

v_{DIFF} is the Differential voltage signal

Eye Height Measurement:

The measured minimum vertical eye opening at the UI center as shown in the plot of the eye diagram. There are three types of Eye Height values:

Eye Height – Transition:

$$V_{EYE-HEIGHT-TRAN} = V_{EYE-HI-TRAN-MIN} - V_{EYE-LO-TRAN-MAX}$$

Where:

$V_{EYE-HI-TRAN-MIN}$ is the minimum of the high transition bit eye voltage at mid UI

$V_{EYE-LO-TRAN-MAX}$ is the maximum of the low transition bit eye voltage at mid UI

Eye Height – Non-Transition:(-3.5 dB and -6 dB)

$$V_{EYE-HEIGHT-NTRAN} = V_{EYE-HI-NTRAN-MIN} - V_{EYE-LO-NTRAN-MAX}$$

Where:

$V_{EYE-HI-NTRAN-MIN}$ is the minimum of the high non-transition bit eye voltage at mid UI

$V_{EYE-LO-NTRAN-MAX}$ is the maximum of the low non-transition bit eye voltage at mid UI

5.2.2 TX De-Emphasized Differential Output Voltage (Ratio) MOI

Test Definition Notes from the Specification:

- This is the ratio of $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 3-11 (Draft Specification. Also refer to the transmitter compliance eye diagram shown in Figure 3-9 (Draft Specification).

$V_{TX-DE-RATIO}$ (De-Emphasized Differential Output Voltage (Ratio)) is defined in Table 3-3 (Draft Specification).

Limits (specified only at transmitter pins compliance test point):

Maximum = -4.0 dB and Minimum = -3.0 dB, and the Pass Condition is

 -3.0 dB $< V_{TX-DE-RATIO} <$ -4.0 dB

Limits (specified only at transmitter pins compliance test point):

Maximum = -7.0 dB and Minimum = -5.0 dB, and the Pass Condition is

 -5.0 dB $< V_{TX-DE-RATIO} <$ -7.0 dB

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **De-Emphasis** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

This measurement is made over the entire data defined in Section 3.4 (Draft Specification). The De-Emphasis measurement calculates the ratio of any non-transition eye voltage (2nd, 3rd, etc. eye voltage succeeding an edge) to its nearest preceding transition eye voltage (1st eye voltage following an edge). In Figure 11, it is the ratio of the black voltages over the blue voltages. The results are given in dB.
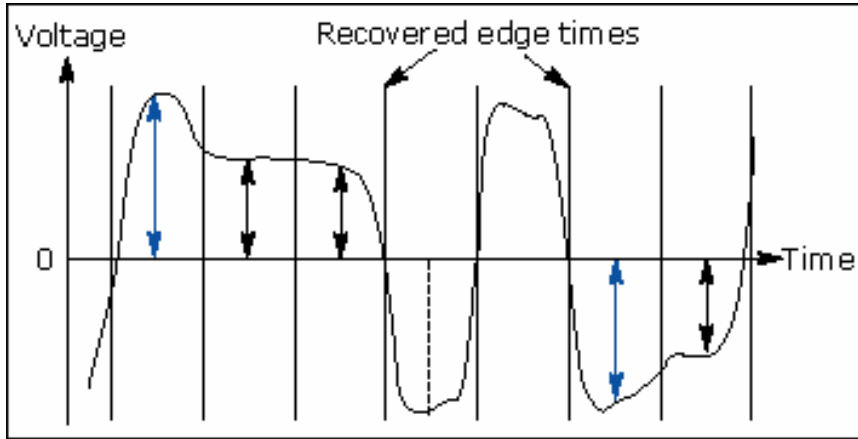

Figure 11: De-emphasis measurement

$$DEEM(m) = dB\left(\frac{v_{EYE-HI-NTRAN}(m)}{v_{EYE-HI-TRAN}(n)} \right)$$

or

$$DEEM(m) = dB\left(\frac{v_{EYE-LO-NTRAN}(m)}{v_{EYE-LO-TRAN}(n)} \right)$$

Where:

$v_{EYE-HI-TRAN}$ is the high voltage at mid UI following a positive transition.

$v_{EYE-LO-TRAN}$ is the low voltage at mid UI following a negative transition

$v_{EYE-HI-NTRAN}$ is the high voltage at mid UI following a positive transition bit

$v_{EYE-LO-NTRAN}$ is the low voltage at mid UI following a negative transition bit

m is the index for all non-transition UIs

n is the index for the nearest transition UI preceding the UI specified by m

5.2.3 Minimum TX Eye Width MOI

Test Definition Notes from the Specification:

T_{TX-EYE} (Minimum TX Eye Width) is defined in Table 3-3 (Draft Specification).

Limits:

Transmitter pins compliance test point: 0.70 UI (218.75ps) $< T_{TX-EYE}$ for 3.2Gb/s rate

Transmitter pins compliance test point: 0.70 UI (175.00ps) $< T_{TX-EYE}$ for 4.0Gb/s rate

Transmitter Pins compliance test point: 0.74 UI (154.0ps) $< T_{TX-EYE}$ for 4.8 GB/s rate (Not in Table 3-3 in the current Draft Specification but will be ratified in the upcoming Draft Specification version).

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **eye width/eye height** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

This measurement is made over the entire TX test pattern defined in Section 4 (Draft Specification).

The *measured* minimum horizontal eye opening at the zero reference level is:

$$T_{EYE-WIDTH} = UI_{AVG} - TIE_{Pk-Pk}$$

Where:

UI_{AVG} is the average *UI*

TIE_{Pk-Pk} is the Peak-Peak *TIE*

5.2.4 TX Output Rise/Fall Time MOI

Test Definition Notes from the Specification:

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 1.1 (Draft Specification) and measured over entire data. Also refer to the Transmitter compliance (Draft Specification).

- Measured between 20-80% at Transmitter package pins into a test load as shown in Figure 1.1 (Draft Specification) for both V_{TX-D+} and V_{TX-D-}

$T_{TX-RISE}$, $T_{TX-FALL}$ (D+/D- TX Output Rise/Fall Time) is defined in Table 3-3 (Draft Specification).

Limits (specified only at transmitter pins compliance point):

Minimum = 30ps

Maximum = 90ps.

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **Rise Time** and **Fall Time** are selected in the **Measurements> Select** menu.

Measurement Algorithm:

This measurement is made over the entire TX test pattern defined in Section 4 (Draft Specification).

Rise/Fall time is limited to only rising or falling edges of consecutive transitions for transmitter measurements. (This test is made on differential or pseudo differential waveforms only). Differential signals Rise/Fall Time show up when you select Differential probe type.

Rise Time: The Rise Time measurement is the time difference between when the V_{REF-HI} reference level is crossed and the V_{REF-LO} reference level is crossed on the rising edge of the waveform.

$$t_{RISE}(n) = t_{HI+}(i) - t_{LO+}(j)$$

Where:

t_{RISE} is a Rise Time measurement

t_{HI+} is a set of t_{HI} only for rising edges

t_{LO+} is a set of t_{LO} only for rising edges

i and j are indexes for nearest adjacent pairs of t_{LO+} and t_{HI+} .

n is a the index of rising edges in the waveform

Fall Time: The Fall Time measurement is the time difference between when the $V_{REF\text{-}HI}$ reference level is crossed and the $V_{REF\text{-}LO}$ reference level is crossed on the falling edge of the waveform.

$$t_{FALL}(n) = t_{LO-}(i) - t_{HI-}(j)$$

Where:

t_{FALL} is a Fall Time measurement

t_{HI-} is set of t_{HI} only for falling edge

t_{LO-} is set of t_{LO} only for falling edge

i and j are indexes for nearest adjacent pairs of t_{LO-} and t_{HI-}.

n is the index to falling edges in the waveform

5.2.5 TX AC Common Mode Output Voltage MOI

Test Definition Notes from the Specification:

$$VTX - CM - AC = \frac{Max|VX \text{ - } D + +VTX \text{ - } D \text{ -}|}{2} - \frac{Min|VTX - D + +VTX - D -|}{2}$$

-Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Draft Specification) and common mode measurements to be performed using a 101010 pattern.

Limits (specified only at transmitter pins compliance point):

VTX-CM-ACp-p L Maximum = 90 mV

VTX-CM-ACp-p R Maximum = 80 mV

VTX-CM-ACp-p S Maximum = 70 mV

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **AC CM Voltage** is selected in the **Measurements> Select** menu.

Note: AC CM voltage is available only when Single-Ended probe type is selected.

Measurement Algorithm:

This measurement is made over the entire data defined in Section 3.4 (Draft Specification).

AC CM Voltage:

The AC Common Mode RMS Voltage measurement calculates the RMS statistic of the Common Mode voltage waveform with the DC Value removed. (After DC is removed, the RMS on what is left equals STD)

$$v_{AC-RMS-CM}(i) = RMS(v_{AC-M}(i))$$

Where:

i is the index of all waveform values

$v_{AC-RMS-CM}$ is the RMS of the AC Common Mode voltage signal

v_{AC-M} is the AC Common Mode voltage signal.

5.2.6 TX DC Common Mode Voltage MOI

Test Definition Notes from the Specification:

Defined as: $VTX - CM = DC(avg)of \dfrac{|VX\text{-}D\text{+}+VTX\text{-}D\text{-}|}{2}$

- Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 4-25 (Draft Specification) and common-mode measurements to be performed using a 101010 pattern. Measured over the entire data. Also refer to the transmitter compliance eye diagram shown in Figure 4-24 (Draft Specification).

Limits (specified only at transmitter pins compliance point):

VTX-CM_L Maximum = 375 mV

VTX-CM_S Maximum = 280 mV and VTX-CM_S Minimum = 135 mV.

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **DC Common Mode Voltage** is selected in the **Measurements> Select** menu.

Note: DC CM voltage available only when you select Single-Ended probe type.

Measurement Algorithm:

This measurement is made over the entire data defined in Section 3.4 (Draft Specification).

The DC Common Mode measurement:

The DC Common Mode measurement returns the average of absolute value of common mode waveform.

5.2.7 TX Waveform Eye Diagram Mask Test MOI

Test Definition Notes from the Specification:

- The TX eye diagram in Figure 3-9 (Draft Specification) is specified using the passive compliance/test measurement load in place of any real FB-DIMM interconnect + RX component.

- Twenty-seven eye diagrams must be met for the Transmitter. The eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

- The eye diagram must be valid for entire TX test pattern as defined in the section 4 of the draft specifications.

For Transmitter Pins Mask Geometries from the Draft Specification, refer to the Figure 1 of this MOI.

5.2.8 TX Dj Dual-Dirac MOI

Test Definition Notes from the Specification:

-Specified at the package pins into a timing and voltage compliance test load. This number does not include the effects of Spread Spectrum Clock (SSC) or reference clock jitter. Defined is the Dual-Dirac deterministic jitter as described in Section 4 of the Draft Specification.

Limits (specified only at transmitter pins compliance point):

Maximum = 0.2 UI. For 3.2 Gb/s and 4.0 Gb/s data rate.

Maximum = **TBD** for 4.8 Gb/s data rate.

Test Procedure:

Follow the procedure in Section 4.4 (Draft Specification), ensuring that **Jitter@BER** is selected in the **Measurements> Select** menu.

Measurement Algorithm: (refer to the same section in RX)

The DJ PDF is composed only of a pair of Dirac delta functions (Dual-Dirac). The Dual-Dirac model is assumed for system, allowing rms RJ Gaussian components to be added with DJ Dual-Dirac component linearly. The Dual-Dirac description is merely the linearization of the CDF (Cumulative Distribution Function) at a particular BER. Since the CDF has two sides, this linearization is performed twice, and the result is then combined. The Tx-Dj is estimated by equivalently deriving the CDF at points where BER $< 10^{-9}$ and Extrapolating ϕ to a BER $< 10^{-9}$, such that a device exceeding the DJ specification is identified with a 99.7% confidence interval.

6 FB-DIMM Reference Clock Compliance Testing

This section provides the Methods of Implementation (MOIs) for Reference clock tests using a Tektronix real-time oscilloscope, probes, the RT-Eye compliance software solution (version 2.0), and with the Tektronix NEX-TDSFBDP test fixture / JEDEC parametric test fixture.

- To reduce jitter and allow for future silicon fabrication process changes, HCSL (**High-speed Current Steering Logic**) clocks are used, as illustrated in Figure 3-1(Draft Specifications). The nominal single-ended swing for each clock is 0 to 0.7 V. The same system clock shall be transmitted to the two components at the ends of the link, if necessary, through connector(s).

- The reference clock frequency is 1/24 of the link data rate, for example: 166.67 MHz for a data rate of 4.0 Gb/s. The reference clock pair is routed point-to-point to each device from the system board.

- The FB-DIMM channel uses mesochronous clocking; the phase relationship between TX reference clock and RX reference clock is unspecified. However, in order to limit the jitter difference between TX and RX there is an upper limit for the phase difference between the data and reference clock at the RX (also known as the transport delay, specified in Table 3-1).

SSC (Spread Spectrum Clock) with up to -0.5% down spread in frequency shall be supported. The frequency of the clock and bit rate can be modulated from **0% to -0.5%** of the nominal data rate/frequency, at a modulation rate between 30 kHz and 33 kHz. The modulation profile of SSC shall be able to provide optimal or close to optimal EMI reduction. Typical profiles include triangular or "Hershey kiss" profile.

6.1 Probing the Link for Reference Clock Compliance

Use probing configuration (B or D) to probe the link differentially at a point close to the pins of the reference clock. Alternatively, use probing configuration (A or C) using the Ch1 and Ch3 inputs of an oscilloscope that has 40 GS/s sample rate available on two channels (TDS6124C and TDS6154C series only).

6.2 Running a Complete Reference clock Compliance Test

The MOIs for each Reference clock test are documented in the following sections. All Ref clock measurements can be selected and run simultaneously with the same acquisition. To perform a compliance test of all receiver measurements:

1. Select **Measurements> Select**.

2. Select **Bit Rate**.

3. Select **Reference clock** from the Test Point pull-down list.

4. Select **Differential** (or Single-Ended) as the Probe Type, depending on your probe configuration.
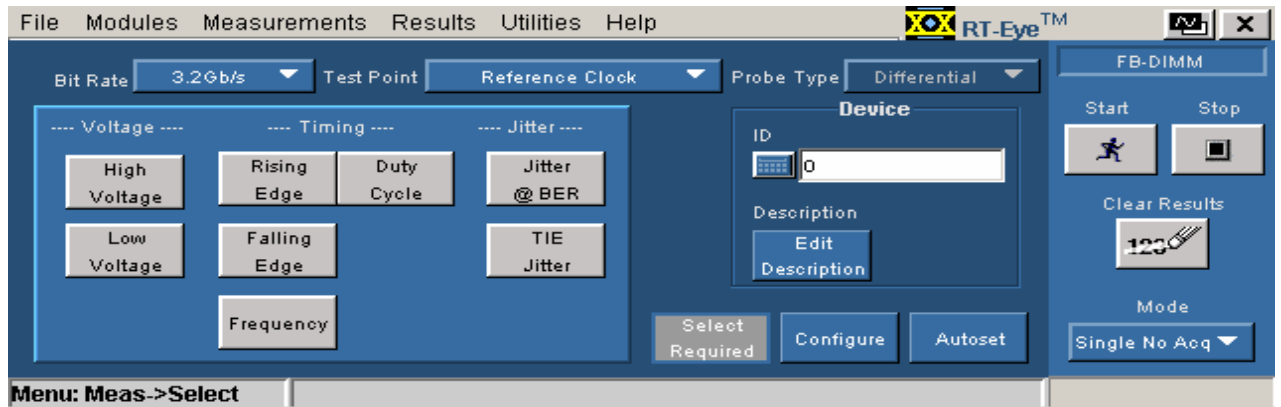
Figure 12: Measurements Select menu setup

5. Click the **Select Required**.

6. Click **Configure** to access the Configuration menus and set up Signal Source.

7. Click **Autoset** to auto set signal and reference levels.

8. Click **Start**.

Figure 13 shows the result of a reference clock compliance test on a signal that passes the Reference Clock tests.
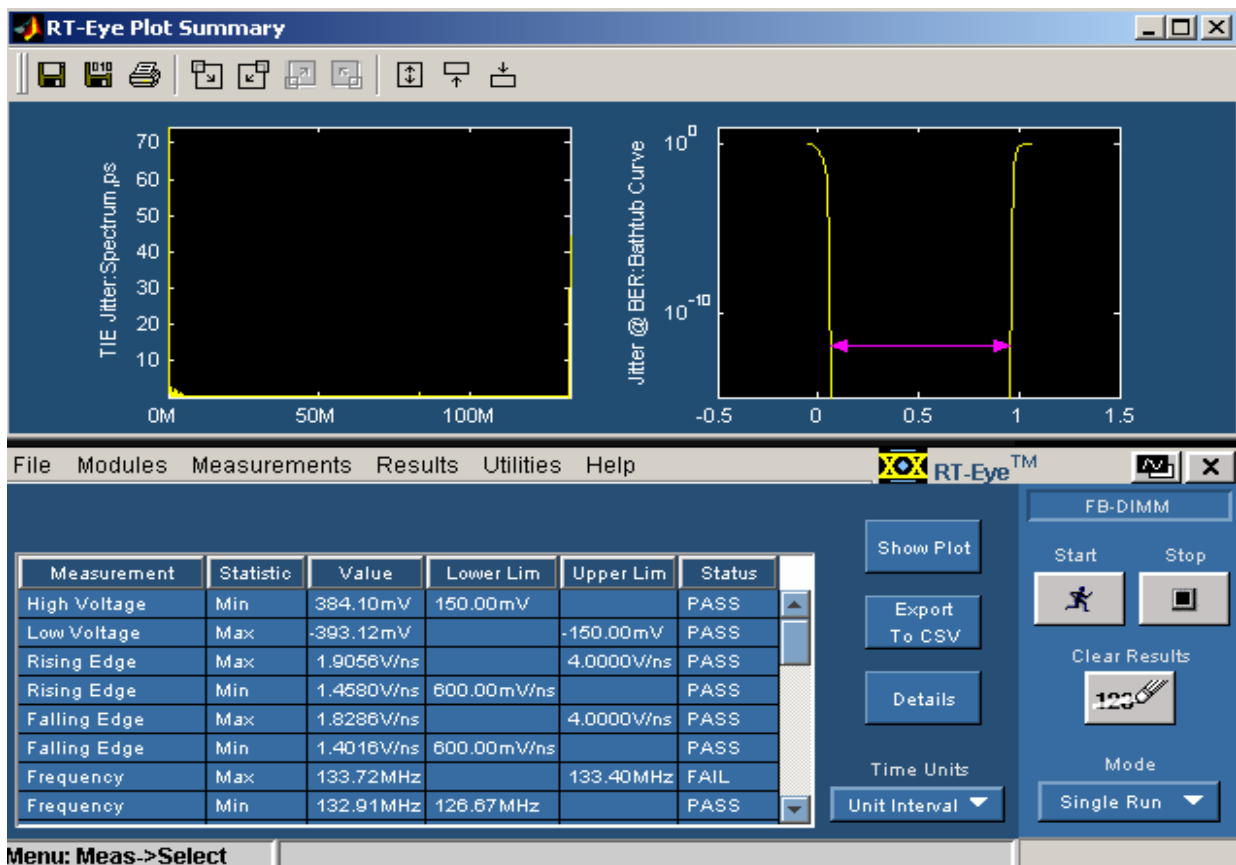

Figure 13: Result of a completed compliance test at the reference clock pins

6.2.1 Reference Clock Frequency Measurement Test MOI

Test Definition Notes from the Specification:

Reference clock frequency is measured for each data rate of operation.

-This is measured with SSC disabled. Enabling SSC will reduce reference clock frequency.

-Compliance to frequency specification is only required for those data rates supported by the DUT.

Limits:

 fRefclk-3.2 : Min = 126.67 MHz ; Max = 133.40 MHz ; Nominal = 133.33 MHz

 fRefclk-4.0 : Min = 158.33 MHz ; Max = 166.75 MHz ; Nominal = 166.67 MHz

 fRefclk-4.8 : Min = 190.00 MHz ; Max = 200.10 MHz ; Nominal = 200.00 MHz

Test Procedure:

Follow the procedure in Section 4.7 (Draft Specification), ensuring that **reference clock frequency** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

The reference clock waveform period is calculated and the frequency is derived from the period measurement.
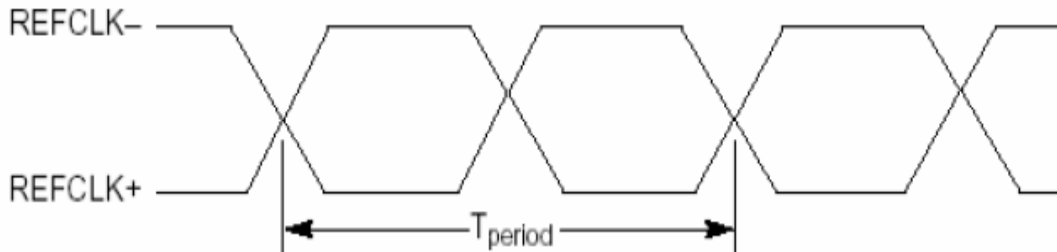
Freq = 1/T period

Figure 14: Reference Clock

6.2.2 Reference Clock Differential Voltage Hi and Lo Test MOI

Test Definition Notes from the Specification:

Differential Voltage Hi and Differential Voltage Lo measurements are taken from differential waveforms.

Limits:

Vref clk- Diff -Hi Minimum = +150 mV.

Vref clk – Diff-Lo Maximum = -150 mV.

Test Procedure:

Follow the procedure in Section 4.7 (Draft Specification), ensuring that **Reference clock differential voltage Hi/Lo** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

Hi voltage < 150 mV = Fail

Lo Voltage > -150 mV = Fail

6.2.3 Reference Clock Differential rise and fall edge rates test MOI

Test Definition Notes from the Specification:

The rising and falling edge rates measurements are taken from differential waveforms.

- Measured from -150 mV to + 150 mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement Window is centered on the differential 0 V crossing.
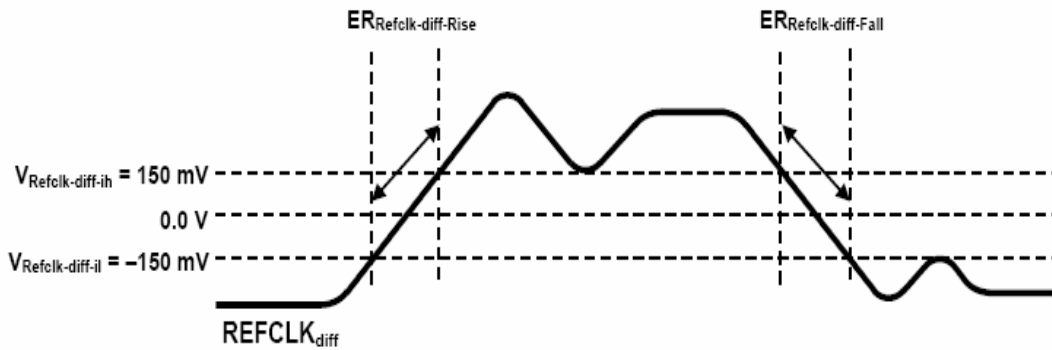

Figure 15: Reference clock rise/fall time calculation

Limits:

Minimum = 0.6 V/ns

Maximum = 4 V/ns.

Test Procedure:

Follow the procedure in Section 4.7 (Draft Specification), ensuring that **Rise Time/Fall Time** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

The rising edge and falling edge are calculated over the 300 mV window, which is centered at differential 0 V. The rising/falling edge rate V/ns = 300 mV/Rise/Fall Time.

6.2.4 Reference clock Duty cycle test MOI

Test Definition Notes from the Specification:

The duty cycle measurement of reference clock is taken from differential waveform.

Limits:

Minimum = 40%

Maximum = 60%

Test Procedure:

Follow the procedure in Section 4.7 (Draft Specification), ensuring that **duty cycle** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

Duty Cycle = positive pulse width / clock period

This is measured at differential 0 V reference voltage level.

6.2.5 Reference Clock Jitter RMS Test MOI

Test Definition Notes from the Specification:

Different devices may have different phase jitter1 tracking behaviors due to variation of the jitter transfer function of their PLLs, transport delays between transmitter and receiver, differences in the propagation delays in the devices and the phase tracking bandwidth of the clock phase recovery circuitry.

For the FB-DIMM channel to function properly when the transmitter and receiver use devices with different phase jitter tracking behavior, a specification of the reference clock jitter spectrum is necessary. To measure jitter on the reference clock and translate this directly into a data eye closure at the receiver, the reference clock phase jitter is filtered by a phase jitter transfer function that represents the worst case mismatch between transmitter and receiver's phase tracking. After convolving this frequency domain filter with the reference clock phase jitter spectrum, the peak-peak jitter is measured in the time domain. As this is a total jitter specification that includes both deterministic and random jitter components, the sample size is also specified to meet the link's BER goal.

- Measured with SSC enabled on reference clock generator
- Measured after phase Jitter filter

Limits:

Maximum = 3 ps.

Test Procedure:

Follow the procedure in Section 4.7 (Draft Specification), ensuring that **Jitter@BER** is selected in the **Measurements> Select** menu.

Measurement Algorithm:

Refer to Specifications section 3.1.3.A second-order PLL transfer function is used as an approximation for transmitter and receiver. Actual PLLs used in typical CMOS processes are often third order or higher order. However, all can be approximated as a second-order transfer function. The transfer function assuming second-order PLLs with PI control loops is defined by the following s domain equation:

$$H(s) = \left[\frac{2s\zeta_1\omega_1 + \omega_1^2}{s^2 + 2s\zeta_1\omega_1 + \omega_1^2} e^{-sT_1} - \frac{2s\zeta_2\omega_2 + \omega_2^2}{s^2 + 2s\zeta_2\omega_2 + \omega_2^2} \right] \left[\frac{s}{s + \omega_3} \right]$$

In this equation, $\zeta 1/2$ are the damping factors for PLL 1 and 2, and $\omega 1, 2$ are the natural frequencies for the PLLs 1 and 2 and $\omega 3$ is bandwidth of the RX clock/data phase recovery circuitry. This function is not meant as a requirement for an implementation. It is used as a bounding function for modeling purposes to establish the limits for f_3 dB frequency and maximum peaking.

7 Giving a Device an ID

The FB-DIMM Compliance Module provides a graphical user interface (See Figure 4) for entering a Device ID and Description. Data entered here will appear on the compliance report and is recommended for device tracking.

8 Creating a Compliance Report

To create a compliance report, select **Utilities> Reports**. The Report Generator utility can create a complete report of the compliance test.